The semiconductor industry is now in its third generation of metal-oxide-semiconductor field-effect transistor (MOSFET) operation. The first generation was silicon dioxide ($\kappa = 4$) for the SiON film technology for the sub-1 nm dielectric constant of the nitrogen containing SiO$_2$ film, and the summation over $\kappa$ is layers that do not have a uniform nitrogen profile. Today, the era of SiON films with an equivalent oxide thickness (EOT) in the range of $\sim 0.1-0.2$ nm have been in mass production for nearly a decade, meeting demanding transistor and reliability requirements. For SiON thickness less than ~1.0 nm, however, it was again demonstrated that direct tunneling leakage currents become excessive through the SiON. Scaling below ~1 nm for higher-performance devices and lower than ~1.5 nm for lower-power devices also became limited by poly-silicon depletion as well as gate dielectric leakage. Initial solutions will require either higher content nitrogen in SiON than currently in production or higher $\kappa$ dielectric constant gate materials ($\kappa > 10$). Serious attention for alternate, higher dielectric constant materials began in 1995 and have resulted in an extensive literature. $\kappa$ Hafnium-based gate dielectrics have emerged as the broad industrial choice for high-$\kappa$ gate dielectric material. The principal motivation for moving to high-$\kappa$ gate dielectrics was the need to reduce direct tunneling gate leakage currents. This was achieved by increasing the dielectric's physical thickness inasmuch as the direct tunneling leakage current is drastically reduced due to its exponential dependence on the physical gate dielectric thickness. Consequently, the gate dielectric constant, $\kappa$, is increased. These two changes result in the approximate constancy of the MOSFET's capacitance, a significant parameter controlling the speed of the device. This is achieved by appropriately modifying the selected gate dielectric constant, $\kappa$, to the dielectric's physical thickness. As a result the MODFET electrically behaves as though its gate dielectric thickness is larger than its physical thickness (to reduce direct tunneling leakage current) by the ratio of the dielectric constant of SiON (generally slightly more than SiO$_2$'s value of $2.0$) but significantly less than the dielectric constant of SiON ($\sim 7.5$) to the higher dielectric constant of the oxide. The silicon dioxide ($\kappa = 1.7$) is the dominant gate dielectric ($\kappa = 15$-20 for the HIO, and $\kappa = 30$-40 for the SiON). This trend regime of gate dielectric technology has also required the replacement of the dielectric layers that do not have poly-silicon gate dielectrics. The selection of materials, and the use of high-$\kappa$ dielectric materials is a very active area of research.

## Silicon Oxynitride

SiON dielectrics were first introduced at an EOT of about 3 nm and at that time required less than about 10 atomic percent nitrogen to minimize boron penetration and gate leakage. Control incorporation of nitrogen, especially concentration and depth profile, was critical to the introduction of SiON. The key process parameter to be controlled in the introduction of the first reliable SiON gate dielectric was the plasma nitridation of SiO$_2$.

The advantage of plasma nitridation of SiO$_2$ is that it is done at a relatively low temperature to avoid any damage to the silicon substrate or the gate dielectric. The principal motivation for moving to high-$\kappa$ gate dielectrics was the need to reduce direct tunneling gate leakage currents. This was achieved by increasing the dielectric's physical thickness inasmuch as the direct tunneling leakage current is drastically reduced due to its exponential dependence on the physical gate dielectric thickness. Consequently, the gate dielectric constant, $\kappa$, is increased. These two changes result in the approximate constancy of the MODFET's capacitance, a significant parameter controlling the speed of the device. This is achieved by appropriately modifying the selected gate dielectric constant, $\kappa$, to the dielectric's physical thickness. As a result the MODFET electrically behaves as though its gate dielectric thickness is larger than its physical thickness (to reduce direct tunneling leakage current) by the ratio of the dielectric constant of SiON (generally slightly more than SiO$_2$'s value of $2.0$) but significantly less than the dielectric constant of SiON ($\sim 7.5$) to the higher dielectric constant of the oxide. The silicon dioxide ($\kappa = 1.7$) is the dominant gate dielectric ($\kappa = 15$-20 for the HIO, and $\kappa = 30$-40 for the SiON). This trend regime of gate dielectric technology has also required the replacement of the dielectric layers that do not have poly-silicon gate dielectrics. The selection of materials, and the use of high-$\kappa$ dielectric materials is a very active area of research.

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criteria were originally established for the formation of low defect density glasses, the maximum average number of bonds (N\textsubscript{O}) of ~3 is the limit for a low defect density dielectric. If a thin SiO\textsubscript{2} layer (~0.5nm, about one molecular layer) is formed between the Si substrate and HfO\textsubscript{2}, cation bonding coordination is reduced to 1.0, and is essentially the same as for the Si-SiO\textsubscript{2} interfaces leading to significantly improved electrical performance. Monolayer-level nitrogen incorporation (\sim 7 x 10\textsuperscript{-10} cm\textsuperscript{2}) to form Si-N\textsubscript{x} bonding configurations in the vicinity of the Si-SiO\textsubscript{2} interface\cite{4} reduces gate leakage by approximately tenfold compared to pure SiO\textsubscript{2} as shown in Fig. 1.\textsuperscript{7} The incorporation of nitrogen near the Si-SiO\textsubscript{2} interface leads to reduced interfacial sub-oxide bonding which defines the transition region between the Si substrate and bulk SiO\textsubscript{2}. The modified interface structure results in the reduction of gate tunneling currents by increasing the tunneling barrier height. Although monolayer level incorporation of nitrogen at the interface improves leakage characteristics, further scaling will require higher bulk nitrogen levels.

Increasing the nitrogen concentration in the bulk of the film by either direct nitridation or nitridation of the SiO\textsubscript{2} base oxide reduces gate leakage. In the case of (SiO\textsubscript{2-x}N\textsubscript{x}), solution, the gate leakage can be reduced by as much as a factor of about 100.\textsuperscript{8} Figure 2 shows leakage current as a function of silicon nitride fraction in SiON.\textsuperscript{9} The leakage reduction is clearly demonstrated for the solid solution in the vicinity of the 50-50% composition point. Further Figure 3 further shows that the leakage current of SiON can indeed be decreased by increasing the nitrogen concentration in SiON to ~20 at.\% as an example. Nitrogen concentrations in excess of ~20 at.\% however, results in large shifts in the threshold voltage which can be observed in both MOSFET and pMOSFET devices with the pMOSFET shift being larger. In addition, the leakage reduction of SiON with high nitrogen is not sufficient for scaling dielectrics beyond the 45 nm technology node and high-x is necessary to meet the scaling requirements.\textsuperscript{10}

High-k Dielectric Constant Materials

The semiconductor community has been searching for high-k gate dielectrics since about 1995. It appears that, after investing in a multitude of materials, Hf-based gate dielectrics have emerged as the “final” choice for high-x material. The primary motivation for moving to high-k gate dielectrics was the need to reduce direct tunneling leakage currents as discussed earlier. Figure 5 shows a comparison of the gate leakage of SiON and hafnium silicon oxynitride (HfSiON) as a function of composition indicating that HfSiON is scalable in the vicinity of the Si-SiO\textsubscript{2} interface. The amorphous nature of HfSiON,\textsuperscript{11} Thus, in general, the idea of creating HfSiON is that hafnium is added to silicon dioxide to increase the dielectric constant and nitrogen is added to stabilize the material structure. An additional challenge observed with HfSiON deposited by atomic layer deposition was large C-V hysteresis for n-channel devices as a result of a high density of trapped charge in the bulk of the dielectric film.\textsuperscript{12} HfSiON on the other hand has shown significantly lower trapped charge than HfO\textsubscript{2} as shown in Figure 5.\textsuperscript{13} Subsequently, improvements in charge trapping were observed for very thin hafnium oxynitride (HfON) on thin SiO\textsubscript{2}, (EOT \leq 1.1 nm) with the improvement being attributed to a lower number of total defects in HfON and the formation of a “silicate” at the interface.\textsuperscript{14} The improvement in charge trapping for the thinner HfON film was also followed by electron mobility improvements (approaching ~90% of the SiO\textsubscript{2} electron mobility at an electric field of ~ 1 MV/cm). The presence of a thin SiO\textsubscript{2} or SiON interface and the addition of Si to HfON have in general been found to improve mobility as shown in Figure 6 and decrease charge trapping.\textsuperscript{15} The industry recognizes the many benefits of HfSiON as a high-k gate-dielectric and devoted considerable resources in order to introduce poly-Si/HfSiON gate stack into the conventional flow. However, pMOSFET with poly-Si gate electrode devices suffered from a high threshold voltage (V\textsubscript{T}) \textsuperscript{16} phenomenon that became known as pMOSFET V\textsubscript{T} offset, threshold voltages offset as high as 3-5 V have been observed.
The incorporation of nitrogen near the SiO₂ interface leads to reduced interfacial sub-oxide bonding which defines the transition region between the Si substrate and bulk SiO₂. The modified interface structure results in the reduction of gate tunneling currents by increasing the tunneling barrier height. Although monolayer level incorporation of nitrogen at the interface improves leakage characteristics, further scaling will require higher bulk nitrogen levels. Increasing the nitrogen concentration in the bulk of the film by either direct nitridation or nitridation of the SiO₂ base oxide reduces gate leakage. In the case of (SiO₂-N), solution, the gate leakage can be reduced by as much as a factor of about 100.  

Figure 2 shows leakage current as a function of silicon nitride fraction in SiON. The leakage reduction is clearly demonstrated for the solid solution in the vicinity of the 30:70 SiO₂:Si₃N₄ composition point. Figure 3 further shows that the leakage current of SiON can indeed be decreased by increasing the nitrogen concentration in SiON to ~20 at. % as an example. Nitrogen concentrations in excess of ~20 at. %, however, results in large shifts in the threshold voltage which can be observed in both SiMESFET and pMESFET devices with the pMESFET shift being larger. In addition, the leakage reduction of SiON with high nitrogen is not sufficient for scaling dielectrics beyond the 45 nm technology node and high-x is necessary to meet the scaling requirements.  

**High-x Dielectric Constant Materials**

The semiconductor community has been searching for high-x gate dielectrics since about 1995. It appears that, after innumerable papers on a multitude of materials, Hf-based gate dielectrics have emerged as the “final” choice for high-x material. The principal motivation for moving to high-x gate dielectrics was the need to reduce direct tunneling leakage currents as discussed earlier. Figure 1 shows a comparison of the gate leakage of SiON and hafnium silicon oxynitride (HfSiON) as a function of composition indicating that HfSiON is scalable even after annealing at temperatures well above the typical nitrogen processing temperature of ~700°C. It is generally agreed that amorphous high-x gate dielectrics are preferred over crystalline materials. For example, hafnium oxide (HfO₂) and hafnium silicon oxide (HfSiO) were key gate dielectrics studied in the early stages of high-x development, but both have relatively low crystallization temperatures. Figure 4a shows a cross-sectional transmission electron micrograph (TEM) of HfO₂ that clearly shows ordering, and indication of crystallization in the film after poly silicon deposition at about 700°C. HfSiO also crystallizes at temperatures lower than the maximum CMOS processing temperatures and, in addition, also suffers from phase separation that results in crystalline HfO₂ phases in a matrix of HfSiO with a lower Hf concentration than the original as deposited uniform HfSiO. These results are less than desirable because polycrystalline films contain point defects and grain boundaries that place significant limitations on the device reliability. Therefore, more thermally stable dielectrics were preferable.

A few research groups have reported that HfSiON is structurally stable, has a high dielectric constant, has low charge trapping, and high electron and hole mobility, typically ~90% and >90% of SiO₂, universal mobility curve at an electric field of 1 MV/cm, for HfSiON having Hf and N concentrations of ~11 at.% and 14 at.%, respectively. The addition of ~14 at. % nitrogen to HfO₂ (~21 at. %) to form HfSiON was found to stabilize the structure of the films such that the material remains amorphous up to 1100°C for low Hf concentrations. Figure 4b shows a TEM micrograph of poly-Si/HfSiON/Si after annealing at 1050°C where no lattice fringes are observed due to the amorphous nature of the films. X-ray diffraction and Fourier Transform infrared Spectroscopy data also support the amorphous nature of HfSiON. Thus, in general, the idea of creating HfSiON is that hafnium is added to silicon dioxide to increase the dielectric constant and nitrogen is added to stabilize the material structure. An additional challenge observed with HfO₂ deposited by atomic layer deposition was large C-V hysteresis for n-channel devices as a result of a high density of trapped charge in the bulk of the dielectric film. HfSiON on the other hand has shown significantly lower trapped charge than HfO₂ as shown in Figure 5. Subsequently, improvements in charge trapping were observed for very thin hafnium oxynitride (HfON) on thin SiO₂, (EOT ~ 1.1 nm) with the improvement being attributed to a lower number of total defects in HfON and the formation of a “silicate” at the interface. The improvement in charge trapping for the thinner HfON film was also followed by electron mobility improvements (approaching ~ 90% of the SiO₂ electron mobility at an electric field of ~1 MV/cm). The presence of a thin SiO₂ or SiON interface and the addition of Si to HfON have in general been found to improve mobility as shown in Figure 6 and decrease charge trapping. The industry recognized the many benefits of HfSiON as a high-k gate-dielectric and devoted considerable resources in order to introduce poly-Si/HfSiON gate stack into the conventional flow. However, pMOSFET with poly-Si gate electrode devices suffered from a high threshold voltage (V_th) a phenomenon that became known as pMOSFET V_th offset, threshold voltages offset as high as 0.5 V have been observed.
Metal Gate Electrodes

As a result of the pMOSFET Vt offset problems in high-k gate stacks, the industry initiated a significant effort to the selection of nMOSFET and pMOSFET metal gate electrode materials in order to obtain low threshold voltages (~0.25 V) and to minimize the depletion effect found in polycrystalline silicon electrodes. Researchers have investigated many metal gate electrode candidates, but the industry has not converged on one set of materials. At present, the poly-Si/HfSiON devices, which require low Vt, seem to be the most promising. Studies of basic methodologies have been pursued to set the metal work function (i.) selection of a metal with appropriate vacuum silicon work function, (ii.) modification of the metal/dielectric interface, and (iii.) modification of the gate dielectric using non-band edge metals. The placement of low work function metals/gates on high-k gate dielectrics at the metal/dielectric interface have been found to lead to enhancements in the work function of the MOSFET and thus Vt of the device but this is also dependent on the thermal budget. The reaction between the dielectric and metals alters the charge in the device, and the work function, and has made setting the work function at the metal/dielectric interface necessary. The nature of the metal/dielectric interface chemistry, the benefits of a lower thermal budget process needs to be considered in order to integrate high-k dielectric/metal stacks into the transistor flow. New approaches such as sacrificial gate dielectrics will usher in the third generation of CMOS gate dielectrics and will enable the sub-1 nm EOT era. Metals gates will replace doped polysilicon gates at the transistor scale to the inversion dielectric thickness to be less than achievable with poly-Si. The sub-1 nm EOT era would not have been possible without the knowledge gained pertaining to the previous generations of SiON and SiO2 dielectrics.

About the Authors

Luigi Colombo is a TI Fellow in the Silicon Technology Development Group at Texas Instruments in Dallas, TX. His areas of expertise and interest include deposition and/or growth of high-k gate dielectric materials, such as SiOxN1−x, high-k gate dielectric applications, ferromagnetic semiconductors, Si0.5Ge0.5 and spinels, and nitrided SiO2. He is the author and co-author of over 125 publications, including 3 book chapters, and holds over 50 U.S. patents. He may be reached at colombo@ti.com.

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References

As a result of the pMOSFET Vt offset problem in practically high-k gate stacks, the industry initiated a significant effort to the selection of nMOSFET and pMOSFET "metal" gate electrode materials in order to reduce low threshold voltages (~0.25 V) and to minimize the depletion effect found in poly-Si electrodes. Researchers have investigated many metal gate electrode candidates, but the industry has not concluded on one set of materials at the present time. The basic methodologies have been pursued to set the work function, (i) selection of a metal with appropriate vacuum level, (ii) modification of the metal dielectric interface, and (iii) modification of the gate dielectric using non-band edge metals.

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