TECH HIGHLIGHTS

Novel Process for Plasma Deposition of Silicon Nitride

Plasma-enhanced chemical vapor deposited (PECVD) silicon nitride, typically deposited at ≤300°C, is widely used as a dielectric material in compound semiconductor devices because of the limited thermal stability of III-V materials. However, due to the low deposition temperature, Si-H and Si-N bonds from the silane and ammonia precursors are not completely broken. Therefore, the resulting silicon nitride typically does not have a fixed stoichiometry, but rather contains varying amounts of Si, N, and H. A research team from the University of Florida, Multiplex, Charles Evans and Associates, Cornell University, and Plasma-Therm has demonstrated a novel technique for preparation of high-quality PECVD silicon nitride films with thermal stability up to 800°C. They achieved excellent film properties by depositing them in a multilayer fashion. In between the deposition of each thin (≤4 nm) silicon nitride layer, they passivated the film by an in situ nitrogen ion plasma treatment. The thermal stability of films as thick as 100 nm was confirmed by refractive index and secondary ion mass spectroscopy (SIMS) measurements. Further evidence of the quality of the films was demonstrated by their extremely slow etch rates (3.5-4.0 nm/min) in hydrofluoric acid based solutions, the slowest ever reported for a low-temperature, plasma-deposited silicon nitride.

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Detection and Mapping of Defects in Organic Coatings

It has been demonstrated recently that local electrochemical impedance mapping (LEIM) and local electrochemical impedance spectroscopy (LEIS) can be used for a real mapping of defects in organic coatings on metal substrates. Researchers at the University of Virginia extended these techniques to detect a wide range of chemical and physical defects in organic coatings. Using a five-electrode EIS system, Wittmann, Leggat, and Taylor showed that five types of chemical and physical defects could be identified using LEIM. These defects are: (1) regions of different dielectric character; (2) regions of increased electrolyte uptake caused by underfilm deposits and absorbed oil; (3) subsurface bubbles; (4) underfilm corrosion; and (5) pinholes. The authors note that "the ability to map the location and make quantitative *in situ* measurements of coating heterogeneities will help identify the source of failure (*i.e.*, coating chemistry, method of application, cure schedule, etc.) and provide insight into the mechanisms of coating degradation."

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Product Selectivity in Hydrogenation Reactions

Partial hydrogenation of alkynes, *via* heterogeneous catalysis using Pt, Pd, or Ni, is important in the industrial synthesis of a variety of organic chemicals. Researchers at Osaka Prefecture University in Japan have reported that electrolytic production of chemisorbed hydrogen on palladium can be used to provide excellent control of both the extent of hydrogenation and the relative yield of the alkeneisomers. They used a two-compartment cell, separated by a 50 µm thick Pd sheet, as the reaction vessel. One compartment was a three-electrode electrochemical cell containing aqueous KOH, with the Pd sheet as the working electrode. The other compartment contained a solution of diphenylacetylene (an alkyne) in tetrahydrofuran. The authors showed that the rate of chemisorbed hydrogen formation (precisely controlled by the applied current) is one key to determining the product distribution. Here, low rates for the production of chemisorbed hydrogen, which then permeates through the Pd to react with the diphenylacetylene, correspond to high yields of *cis*-stilbene (the alkene) compared to bibenzyl (the alkane). The authors hypothesize that this is because the release of *cis*-stilbene from the Pd surface is faster than its reaction with chemisorbed hydrogen. In contrast, high electrolysis currents increased the extent of hydrogenation, with an increase in the relative yield of bibenzyl.

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Treatment of Chemical Mechanical Polishing Waste

Chemical mechanical polishing (CMP) has emerged as a preferred technology for planarization of interlevel dielectrics and metal interconnects in the fabrication of advanced integrated circuits. In CMP, a silicon wafer is pressed onto a rotating pad with polishing slurry flowing between the wafer and the pad. Dielectric films (*e.g.*, SiO_2) are typically planarized using highly alkaline, silica-based slurries. Acidic, alumina-based slurries are used in CMP of metal films (*e.g.*, Al, W, and Cu). It has been estimated that 30-50 liters of slurry waste are generated for each level of planarization of a 200 mm wafer; therefore, the problem of slurry waste treatment is receiving increased attention. Researchers at the University of Arizona recently reported the results of electrophoretic methods for separation of colloidally stable particles from slurry suspensions. Electrodecantation, which results from charged particles migrating toward the electrode of opposite charge, was found to be the controlling mechanism in the clarification of low conductivity silica suspensions. Electrocoagulation, the reaction of negatively-charged slurry particles with positively-charged ions produced by dissolution of the electrode, was shown to clarify high conductivity alumina suspensions. The limits of usefulness and applications of these methods in actual wafer fabrication facilities, as well as additional work needed to scale these batch methods up to continuous waste treatment or recycling processes, are discussed.

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Ultrathin GaAs-on-Insulator Structures

Materials and processes for the fabrication of heterostructure devices, *e.g.*, high electron-mobility transistors (HEMTs) and heterojunction bipolar transistors (HBTs), are currently the subjects of numerous research groups. One of the key areas of investigation is the development of substrate structures for use as templates for the fabrication of lattice-mismatched heteroepitaxial layers. Researchers at the University of Wisconsin-Madison and Epitronics have reported the fabrication and characterization of ultrathin (10 nm) GaAs-on-insulator substrates. They formed the substrates by a bond-and-etchback approach, using a template wafer consisting of borosilicate glass deposited onto a GaAs wafer, and an etch-stop wafer consisting of an alternating, multilevel AlGaAs/GaAs heterostructure. Following wafer bonding at 550°C, the sacrificial GaAs and AlGaAs layers were etched away, leaving only a 10 nm thick GaAs layer on the template wafer. Characterization of this surface layer by atomic force microscopy (AFM) indicated the as-prepared surface morphology is unsuitable for subsequent epitaxial growth. However, a self-limiting oxidation/etching method for improving the surface morphology was confirmed by AFM.

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