INTEGRATION OF MOLECULAR COMPONENTS INTO SILICON MEMORY DEVICES

BY WERNER G. KUHR

Consumer and business appetite for electronic devices drives the semiconductor industry's need for miniaturization. The state of the art of semiconductor devices now has critical feature dimensions substantially less than 0.1 μm.[1] While many devices can be manufactured effectively at such dimensions through the continued extension and optimization of existing process technologies, it is uncertain at what point along the path of miniaturization such devices, which rely on the bulk properties of materials, will retain the required functional characteristics. Much work has been done in the field of molecular electronics, where many investigators have attempted to mimic transistor properties in molecular systems.[1] While the creation of a molecular transistor has received the lion's share of attention (and criticism),[2] transistor fabrication is expected to scale to 10 nm dimensions, albeit with a great deal of effort.[3] Indeed, the component that is most urgently in need of replacement for most semiconductor devices is the charge storage device, *i.e.*, the capacitor.

Almost all existing memory devices utilize charge storage as the mechanism of information storage [including dynamic random access memory (DRAM), FLASH RAM, and one-transistor static RAM (1T SRAM)]. In particular, DRAM consists of large arrays of storage cells, each of which consists of one capacitor and one transistor, where the charge stored on the capacitor indicates the bit level (Fig. 1). Due to the combination of stringent requirements for data fidelity for RAM (which impacts the minimum amount of signal that must be available from each cell for sensing, currently ~100 fC or ~600,000 electrons) and that capacitors are imperfect, leaky devices (the charge on an existing DRAM capacitor decays rapidly, ~100 ms in existing devices), the data stored in each location must be refreshed periodically by reading it and then writing it back again. The frequency at which this refresh must be repeated is determined by many factors, including the magnitude of charge stored in each device (which, in turn, is based on the voltage and the capacitance available), and the leakage current, along with the number of memory elements that must be refreshed in each cycle. Thus, a key design feature in the miniaturization of DRAM circuit elements is the amount of available charge in each capacitor as feature size shrinks.

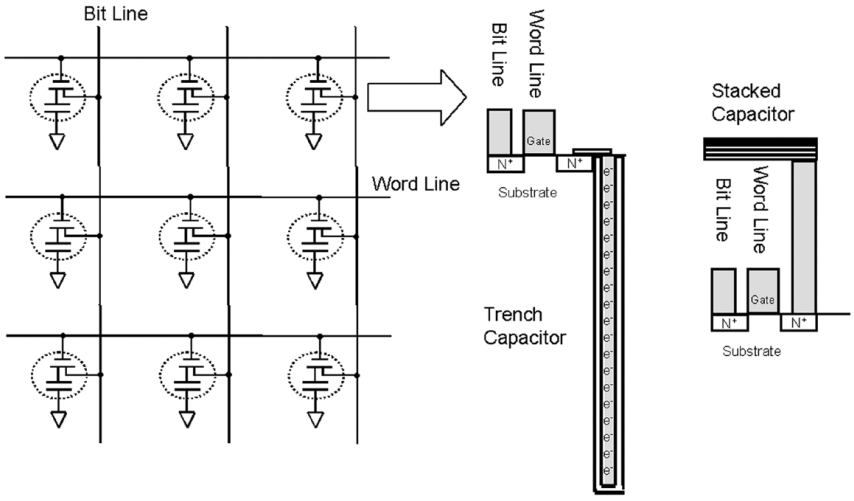

FIG. 1. DRAM array (left), with examples of trench and stacked cell geometries for the DRAM capacitor.

There is increasing evidence that the materials used in existing devices are unable to scale effectively with the other circuit elements used in DRAM circuits. For example, a DRAM capacitor in an efficient memory array must occupy a surface area corresponding to less than $4F^2$ (allowing for a $6F^2$ total cell area), where F is the minimum critical feature size of the device. In a 256 MB DRAM manufactured at the state of the art in a production environment, F is 0.11 μm, and this translates to a capacitor area of roughly 0.048 μm^2, and this cell must be able to operate at less than 2 V. The most commonly used dielectric materials used for DRAM capacitors have a charge density of 1-2 $\mu C/cm^2$, and at these dimensions hold only 1 fC, (roughly 6000 electrons).

Therefore, a tremendous amount of time and effort has been expended by the memory industry to develop three-dimensional structures to provide enough capacitive area to store sufficient charge to allow reliable operation. With a SiO_2 capacitor, almost 5 μm^2 of surface area is necessary to store ~100 fC of charge. Two of the most commonly employed strategies to increase the effective area of the capacitor include trench or stacked structures (Fig. 1). In the trench design, a hole is drilled into the silicon substrate at the critical dimension, and the capacitor is built through deposition of the dielectric on the walls of the cylindrical hole. This can increase the effective area to over 5 μm^2 and provide sufficient capacitance for a reliable device, but at significant manufacturing cost. In this device, the aspect ratio (depth/width) of the trench can be over 100, leading to tremendous process complexity and cost. Fabrication of the DRAM capacitor in existing devices already requires over one-third of the process steps, and this process complexity will increase even more as the aspect ratio becomes larger with even smaller devices. As critical dimensions continue to shrink, it is likely that this process cannot reasonably continue. As discussed in this article, a DRAM based on

Table I. Criteria for Incorporation of Molecules in CMOS Storage Devices.

Property	Implementation
Chemical stability	Delocalized cationic charge
Thermal stability	Decomposition > 400° C
Endurance	Endurance > 10^{12} to 10^{15} cycles
Read/write speed	$t_{R/W} = 1/k_{eff} < 10$ ns
Charge retention	$t_{1/2} > 10$ s
Charge density	$\mu = 10$ μC/cm^2 or higher
Self-assembly and self-alignment	Selective, covalent bond formation of molecules to specific substrate

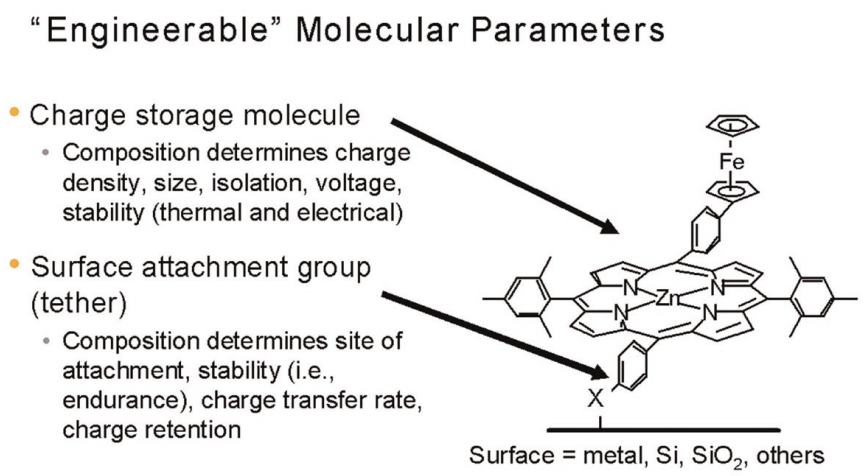

Fig. 2. Properties of molecules used for charge storage.

molecular properties is more suitable for smaller feature sizes.

CHARGE STORAGE IN REDOX MONOLAYERS

Recently, molecules that may be suitable for use in semiconductor devices have been the subject of much attention.[4,5] To be able to serve in this role, molecular components must remain robust under the same daunting conditions that all existing semiconductor materials already endure including high-temperature processing steps during manufacture and demanding requirements for operation (see Table I). There has been considerable skepticism whether molecular materials possess adequate stability, endurance, and operating properties to meet such requirements, and only recently has it been demonstrated that some molecular materials may be able to withstand these demanding criteria.[4] Some redox systems have been investigated for use in the fabrication of molecular-based information storage systems. These systems employ metallocene, porphyrin, and triple-decker sandwich coordination compounds as the charge-storage elements covalently attached to metals and device-grade silicon (Fig. 2).[4-11]

These molecules exhibit redox characteristics that make them amenable for use as multibit information-storage media. Some key aspects of this technology are reviewed below.

- The charge storage properties are dependent on the molecule, not the underlying substrate.[4-11]
- The size of the device dictates the number of molecules (proportional to area).
- Charge is stored in stable redox states of molecules, leading to high charge density (more than ten times higher than conventional SiO_2 capacitors).[4-10]
- Charge-retention times are also a molecular property, not dependent on the leakage characteristics of the gating device, and are in the range of minutes to hours (>10,000 times that of semiconductors).[9]
- Molecules can be attached at high surface coverage (in the range of 1.0×10^{-10} mol cm^{-2}) using small amounts of materials.[8-10]
- Temperatures as high as 400°C can be used during fabrication with no degradation of the molecules. This result is of importance in that many processing steps in fabricating complementary metal-oxide-semiconductor (CMOS) devices entail high-temperature processing, even at the back end of the line.[4]
- Devices using porphyrins applied in this manner have been tested for endurance, and no sign of degradation of any aspect of performance was observed after 10^{12} cycles.[4]
- Multiple bits can be stored in a given memory location using the distinct oxidation states of the molecules, which can lead to higher array densities.[8]
- This type of molecular memory should scale to near molecular dimensions, because electronic properties are intrinsic to the molecular structure.[4-11]

ATTACHMENT OF MOLECULES TO SILICON DEVICES

The fabrication of stable and reliable CMOS/molecular devices requires the covalent attachment of an electroactive molecule (such as a porphyrin or a ferrocene) to a device substrate (*e.g.*, Si). Attachment of molecules to silicon is accomplished through covalent linkage chemistries involving the formation of Si-C or Si-O bonds.[5-11] It is important to emphasize that the stability of the bond formed between the substrate and the redox molecule will dictate the

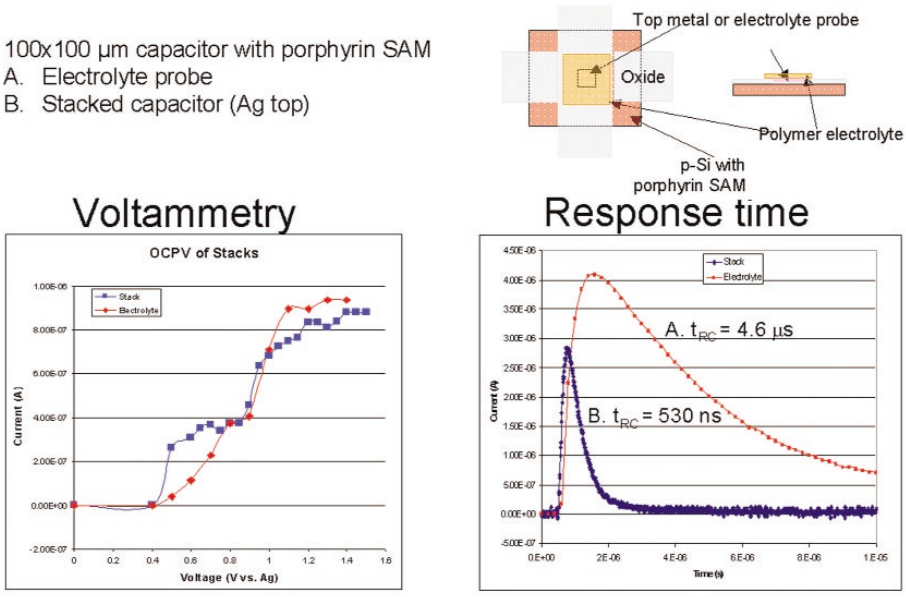

FIG. 3. Hybrid CMOS/molecular DRAM cell.

thermal and electrical stability of the self-assembled monolayer (SAM). For example, thiol/gold chemistry, which has been used extensively in many academic labs for the characterization of monolayer redox systems, does not provide sufficient stability for a robust, manufacturable solution. A number of simple, rapid, material-conservative methods have been examined in our laboratories to attach electroactive molecules to silicon and many other substrates.[5-11] The types of molecules and linkers span a broad range (Fig. 2) and many of these procedures have been published previously.[7-10] The procedures vary considerably depending on the type of molecule and the substrate used for attachment.

A prototype CMOS/molecular DRAM capacitor cell can be manufactured via a straightforward modification of the DRAM architecture, where two metal or semiconductor layers are separated by an electrolyte layer (see Fig. 3). Here, the active area of the molecules is lithographically defined by patterning a field oxide region over the conductive substrate. Many redox systems, some comprised of surprisingly large molecular architectures, have been found to form excellent quality SAMs on silicon.[8-10] Once the molecules are attached, a standard electrochemical cell (which uses a liquid electrolyte and a silver reference electrode) can be used for characterization.[4-10] Alternatively, we can create devices which closely resemble capacitor structures by substituting a thin layer of polymer electrolyte for the dielectric material conventionally used in capacitors, followed by deposition of a metal layer, which is evaporated or sputtered on to complete the cell (Fig. 3). This material can be any well-behaved electrochemical counter electrode material such as copper, silver, etc.

CHARACTERIZATION OF REDOX SAMS IN SILICON DEVICES

The electrochemical properties of redox molecules attached to silicon devices can easily be monitored with traditional electrochemical methods such as cyclic voltammetry or ac impedance.[9] A more relevant measurement for memory devices involves the determination of the charge retention properties of the molecular "capacitor". In this measurement, the porphyrin SAM is oxidized with a short positive voltage pulse (similar to chronoamperometry; roughly 5 × RC time constant (t_{RC}) of the cell) that is ~200 mV above the formal potential of the desired state. The applied potential is disconnected from the counter electrode for a period of time and this disconnection time is varied to evaluate the charge-retention properties of the cell. The charge-retention time can be measured by successively changing the disconnect time up to a point where essentially all the molecules that were initially oxidized have decayed back to the reduced state.[5,9] Measurement of the charge retention times of some redox species has indicated several clear trends. There appears to be little dependence of charge-retention behavior on the substrate size or material, but a strong dependence on the composition and size of the tether separating the redox site from the surface.[9,10] The charge retention time could be increased by an order of magnitude (to over 1000 s) for the same redox species at the same surface, merely by lengthening the tether by three carbons.[9]

The instantaneous current (Fig. 3, right) represents the instantaneous reduction of the charge stored in the oxidized SAM, and the time constant reflects either the t_{RC} of the cell (as when an electrolyte probe is used with a 10,000 µm^2 cell, curve A) or the time constant of the amplifier used for measurement (as shown for the "stacked capacitor", curve B). This signal can be integrated to calculate the total charge remaining, which, in turn, is proportional to the number of molecules that remain oxidized on the surface while the circuit is open. This technique, termed open-circuit potential amperometry (OCPA),[9] has been used to measure charge-retention characteristics of many redox species. This technique can provide voltammetric information as well (OCPV),[9] simply by stepping the write voltage to incrementally larger potentials, and measuring the charge retained (Fig. 3, left). As shown, the OCPV signal looks much like a steady-state voltammogram, where the $E_{1/2}$ of each state is clearly defined. In other experiments, we have characterized the ultimate speed at which the charge can be written or read. For most systems that we have studied, the intrinsic electron-transfer rate constant, or

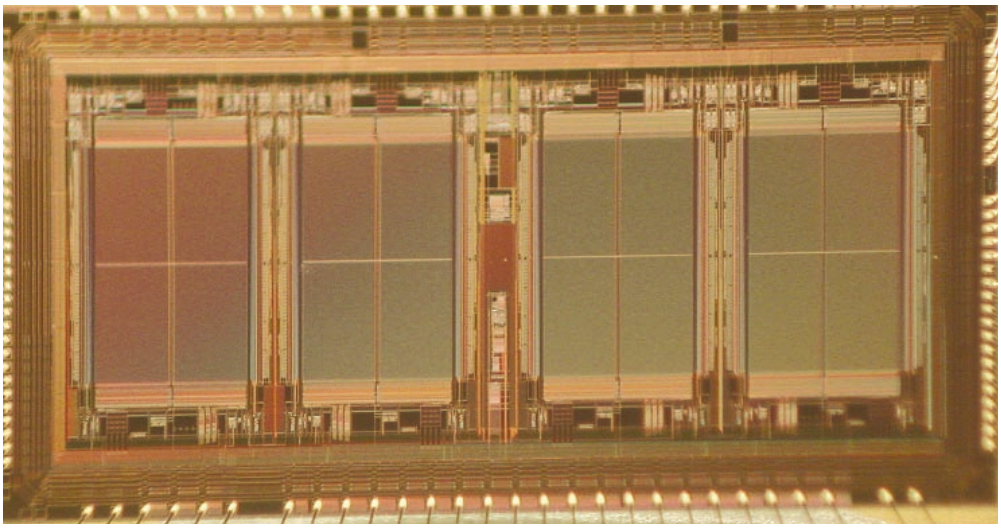

FIG. 4. Photomicrograph of 1 MBit ZettaCore hybrid CMOS/molecular DRAM.

k_o, is sufficiently fast to allow read/write times of a few nanoseconds with a modest overpotential.[9]

HIGH-DENSITY HYBRID MOLECULAR-SILICON DRAM

The true commercial viability of any alternative approach to traditional semiconductor process flow can be demonstrated only through fabrication of devices at densities and scales that approach commercially relevant scales. We have fabricated a prototype 1 Mbit DRAM chip, which incorporates 4 × 256 Kbit arrays of hybrid silicon/molecular capacitors (Fig. 4). While the CMOS circuits were fabricated on a 0.35 µm process flow (to avoid the extremely high mask costs associated with smaller lithography nodes), the DRAM capacitors within these arrays were designed with an area of 0.5 μm^2, roughly an order of magnitude smaller in area than those in existing commercial devices, yet are able to store the same amount of charge as those larger devices. Because the underlying substrate for a hybrid molecular-silicon DRAM can be constructed through use of standard CMOS fabrication technology for all other circuit structures, the only variation in the process occurs at the back end of the line, where the hybrid molecular/silicon structures are formed.

The storage array consists of memory cells arranged in a typical array of transistors and capacitors used in DRAM, each accessed by activation of the proper set of word lines and bit lines (Fig. 4). Each word line is connected to the transistor gating the capacitors of the memory cells in a row, while each bit line is connected to the drains of the memory cells in a column. Peripheral circuits, consisting of row and column decoders, voltage/current/timing generators, and sense amplifiers, are all implemented with CMOS to provide a sensing circuit with timing in the nanosecond regime. It is important to note that the area and the RC delay can be significantly reduced in future CMOS technologies, allowing for even faster operation. While the process that creates the molecular memory array is proprietary, it consists of less than 10% of the number of steps used in the commercial fabrication of DRAM trench capacitors, and is completely compatible with fabrication tools used in commercial foundries today. Each array within this device includes a row of standard SiO_2 capacitors, so that we can simulate, test, and compare their performance with our molecular memory structures. Full testing of this device is currently underway (*e.g.*, including Shmoo to determine operating margins, bit maps to differentiate single bit defects from gross problems, validation on commercial memory testers, and verification of a large number of ac and dc parameters), and initial results are encouraging. The overall performance of the device is expected to be equivalent to or exceed high-speed DRAM devices on the market today.

The fabrication of this kind of test device is an important step in the development of any new technology, and represents the first step in the process of commercial development. It is important to balance the flexibility and robustness of the approach, because this device must serve many purposes, *i.e.*, demonstration DRAM as well as R&D test platform. We want to examine characteristics of many different molecules, for example, by altering the length and type of linker to the porphyrin or by altering the charge storage properties of the molecule. This device gives us tremendous flexibility in characterizing and optimizing the properties of the charge storage molecules as well as the peripheral circuitry, and should allow us ultimately to address many different memory devices and configurations. ■

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