Silicon-Based Electronics: A Series of Perspectives

In organizing the following series of perspectives on silicon-based electronics, we have deviated from our usual magazine format of running individual feature articles. Thus this 'mega-feature' has been divided into three sections: historical background, state-of-the-art, and future directions. These sections in turn contain comments from selected experts on a total of ten sub-topics, which taken together as a unit, provide a useful snapshot of where silicon-based electronics came from, where the field is now, and where it may be heading. Interface *would like to thank Howard Huff, who enthusiastically served as the guest editor for this issue. Huff is well-known to many in the silicon community, and is the driving force behind the quadrennial ECS symposium on Semiconductor Silicon.*

Moore's Law: Beyond Planar Silicon CMOS and into the Nano Era

by Howard R. Huff

The integrated circuit (IC) was invented in 1958 by Jack Kilby of Texas Instruments (mesa process with germanium) and Bob Noyce of Fairchild (planar process with silicon). It was not until the mid to later 1960s, however, that the bipolar IC, and then in the early 1970s, the MOSFET IC, significantly entered the production scene. Patrick Haggerty's vision at Texas Instruments of the pervasiveness of the silicon microelectronics revolution, the concept of the "learning curve," (*i.e.*, the concomitant reduction in the cost of fabrication with the increased volume of production) and market elasticity in the early 1960s was of immeasurable significance to the fledgling IC industry. Concurrently, Gordon Moore's remarkably prescient assessment in 1965 of memory component growth, initially based on bipolar and then MOS memory density, projected that a semi-log graph of the number of memory bits in an IC, versus the date of initial availability, was a straight line, representing almost a doubling per year. Moore's insight (updated at Intel in 1975 to about 18 months and subsequently re-affirmed in 1995) gave impetus to the industry that a viable market was indeed practical. This analysis has become enshrined as Moore's law and became the guiding principle by which the growth of our industry is measured in, *e.g.*, the International Technology Roadmap for Semiconductors (ITRS). These business oriented issues, more-over, coupled with Bob Dennard's one-transistor/one-capacitor dynamic random access memory cell (DRAM) at IBM in 1968, and the related scaling methodologies introduced by Dennard in 1972, established the paradigm by which enhanced scaling has progressed and facilitated the explosive growth and application of the MOSFET IC and the subsequent planar silicon CMOS era.

Historical Background—Implicit in these analyses, viable for about the past 45 years, and clearly anticipated to be the driver for the next 15 years or so, is silicon, its unique oxide and silicon-based technologies such as silicon-germanium and related group IV structures. Robert Cahn presents his historical perspective of silicon and the silicon revolution in an enchanting introduction to the first section. The phenomenal growth of the IC industry, achieved by maintaining Moore's law, is then discussed by Dan Hutcheson.

State-of-the-Art—The characterization, annihilation, and in some cases, the selective utilization of defects to achieve superior IC performance, yield, and reliability is a key cornerstone of our industry. Because many of the phenomena discussed are structure-sensitive, the "process-structure-property" approach continues to be the unifying principle in describing IC electronic characteristics. That is, the fabrication process determines the material structure, which then determines the material properties and subsequent IC electronic characteristics. In that regard, Jim Chelikowsky notes that "computers built with silicon can be used to solve for the electronic properties of silicon itself." Chelikowsky reviews these computational approaches from first principles. Stefan Estreicher continues this first principles study of point defects in silicon. These theoretical considerations, in combination with microscopic experiments, have led to an understanding of silicon incomparable to that of any other material studied in the technological revolution. The selective utilization of defects, as-grown in the silicon crystal as well as process-induced during device/IC fabrication and their mutual interactions, has been used to achieve superior IC performance. Andrei Istratov and Eicke Weber illustrate several aspects of these phenomena. Surely, materials are the *sine qua non* of electronic devices and circuits.

The theme of defects and their control may be further extended by realizing that the surface itself may be considered a giant defect, as noted by H. C. Gatos and others in the 1960s. The characterization and control of the silicon surface is fundamental for stable device and IC characteristics. Yves Chabal and Len Feldman discuss several aspects of the silicon surface and its unique position in silicon microelectronics.

Finally, this section concludes with a summary by Patricia Mooney on current trends in silicon-based nanoelectronics, in particular enhanced carrier mobility. The benefits of utilizing variously configured sequential combinations and compositions of silicon-germanium, to produce strain in the top silicon surface (where the transistor is fabricated), facilitates electron and

Dedication

This snapshot of the IC industry and several opportunities for enhanced growth in the coming nano era is dedicated, in memoriam, to Gary Heerssen, Senior Vice-President of Corporate Manufacturing at Advanced Micro Devices.

hole mobilities beyond the theoretical universal mobility curve. Further materials opportunities are noted inasmuch as an NMOS [PMOS] transistor exhibits optimal electron [hole] mobility for the (100) [(110)] wafer orientation (in the <110> direction for both surfaces). One method of fabricating materials structures to enhance both NMOS and PMOS performance is described as a hybrid orientation technology (HOT) as well as super hybrid orientation technology (SHOT).

Future Directions—The final section of this perspective focuses on evolving issues and opportunities. Tsu-Jae King discusses a host of silicon-based advanced transistor structures and materials, as well as fabrication methodologies in her perspective. King notes that these efforts are expected to extend the ITRS to a physical channel length well below 10 nm, depending on the leakage current specification and power-supply voltage. Konstantin Likharev then discusses a possible role for beyond silicon-based materials opportunities. In this instance, it is anticipated that a single-electron transistor will be operated in conjunction with a CMOS logic IC at room temperature (an extremely important requirement), thereby enhancing the advanced logic CMOS devices beyond what they could achieve on their own. Finally, Ted Kamins discusses alternative bottom-up approaches for device fabrication in the "nano world."

Perhaps our IC industry has been best described by Gordon Moore, who recently noted that "…you are once again reminded that this is no longer just an industry, but an economic and cultural phenomenon, a crucial force at the heart of the modern world." Moore has further noted that "no exponential is forever: but 'forever' can be delayed," which may indeed depend on a new generation of research personnel to maintain, and perhaps, expand the pace of Moore's law in the nano world. ■

About the Author

Howard Huff is a Senior Fellow at SEMATECH. His current responsibilities include issues related to alternative gate stack materials and non-classical CMOS devices. He is co-chair of the Starting Materials Section of the International Technology Roadmap for Semiconductors (ITRS). He is also co-author of the recently published book, High Dielectric Constant Materials: VLSI MOSFET Applications. *He is a Fellow of ECS and the American Physcial Society. He may be reached at howard.huff@sematech.org.*