CMOL: A Silicon-Based Bottom-Up Approach to Nanoelectronics

by Konstantin K. Likharev

The current VLSI paradigm based on a combination of lithographic patterning, CMOS circuits, and Boolean logic (outlined in the first part of this article), can hardly be extended into a-few-nm region. The main reason is that at physical gate lengths below 10 nm, the sensitivity of parameters (most importantly, the gate voltage threshold) of silicon field-effect transistors to inevitable fluctuations in fabrication process parameters increases exponentially; see, *e.g.*, Ref. 1. As a result, the physical gate length should be controlled with a few-angstrom accuracy, far beyond not only the current capability of the semiconductor industry, but its long-term plans as well.[2] Even if such accuracy could be technically implemented using sophisticated patterning technologies, this would probably send the fabrication facilities costs (growing exponentially even now) skyrocketing, and lead to the end of the exponential ("Moore's law") progress of microelectronics some time during the next decade.

The main alternative nanodevice concept, single-electronics,[3,4] offers some potential advantages over CMOS, including a broader choice of possible materials. Unfortunately, for room-temperature operation, the minimum features of these devices (single-electron islands) should be below 1 nm. Since the relative accuracy of their definition has to be between 10 and 20%, the absolute fabrication accuracy should be of the order of 0.1 nm, again far too small for the current and realistically envisioned lithographic techniques.

This is why there is a rapidly growing consensus (see, *e.g.*, Ref. 2) that the impending crisis of the microelectronics progress may be resolved only by a radical paradigm shift from lithography ("top-down") to "bottom-up" fabrication. In the latter approach, the smallest active devices should be formed in a special way (for example, synthesized chemically), ensuring their fundamental reproducibility. An example of such a unit is a specially designed and synthesized molecule comprised of a few hundreds of atoms, including the functional parts (*e.g.*, electron acceptor groups working as single-electron islands and short fragments of non-conducting groups as tunnel junctions); the groups enabling chemically-directed self-assembly of the molecule on pre-fabricated electrodes (*e.g.*, thiol or iso-cyanide groups[5,6]), and probably some additional groups ensuring sufficient rigidity and stability of the molecule at room temperature. The recent experimental demonstration of single-molecule, single-electron transistors by sev-eral groups,[7-11] gives hope for the practical introduction, within the next 10 to 20 years, of the first integrated circuits with such molecular devices.

Unfortunately, integrated circuits consisting of molecular devices alone are hardly viable, because of limited device functionality. For example, the voltage gain of a 1-nm-scale transistor, based on any known physical effect (*e.g.*, the field effect, quantum interference, or single-electron charging), can hardly exceed one,[4] *i.e.*, the level necessary for sustaining the operation of virtually any active analog or digital circuit. This is why I believe that the only plausible way toward high-performance nanoelectronic circuits is to integrate molecular devices, and the connecting nanowires, with CMOS circuits whose (relatively large) field-effect transistors would provide the necessary additional functionality, in particular high voltage gain. Recently, several concrete proposals of such circuits were published (for a recent review, see Ref. 12), and several groups have made initial steps toward the experimental implementation of semiconductor-molecular hybrids.[13-15] Some of the proposals, however, seem either unrealistic, or inefficient, or both; for a discussion, see Ref. 16.

Figure 1 shows our concept of the CMOS/molecular hybrid circuits, dubbed "CMOL".[4,16] Such a circuit combines an advanced CMOS subsystem with two, mutually perpendicular, arrays of parallel nanowires and similar molecular devices formed at each crosspoint of the nanowires. The reason for this topology is that parallel nano-wire arrays may be fabricated by several innovative patterning technologies,
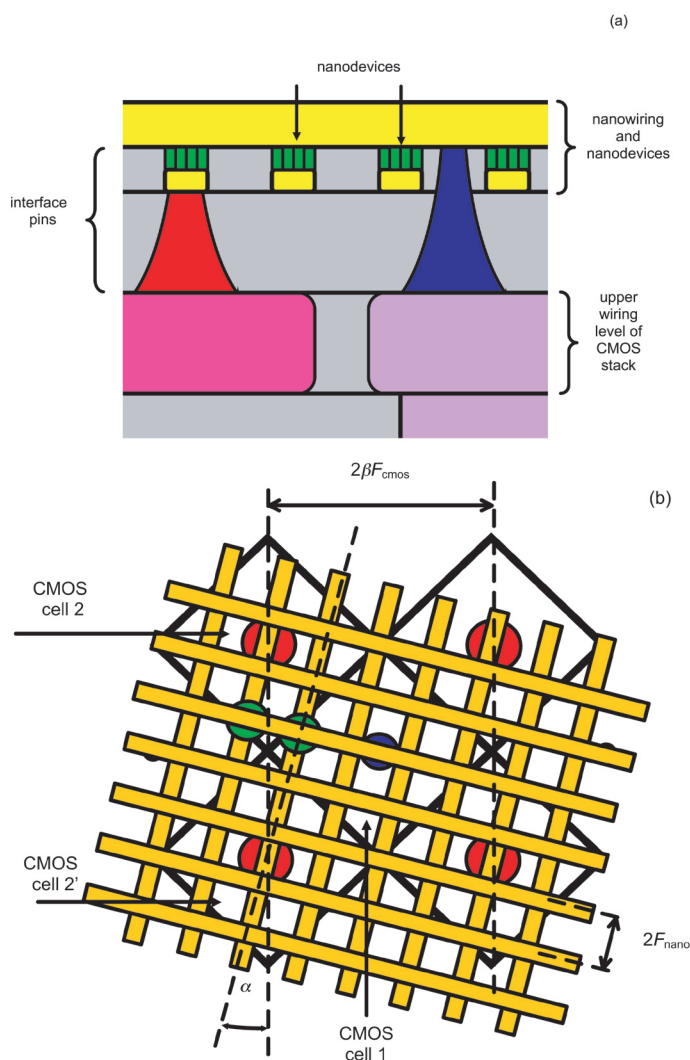
FIG. 1. General structure of a CMOL circuit: (a) side view and (b) top view (schematically). For the sake of clarity, panel (b) shows only five adjacent CMOS cells and two nanodevices. (A similar device is formed at each nanowire crosspoint).

such as nanoimprint[17] or interference lithography,[18] which potentially can provide a-few-nanometer features, at modest cost. These technologies cannot be used for patterning of arbitrary integrated circuits, because they lack adequate layer alignment accuracy, but the crosspoint topology does not require such alignment.

In contrast with the earlier suggestions of crossbar-like hybrid circuits,[12] in CMOL chips, the interface between the CMOS and nanowire/nanodevice subsystems is provided by pins that are distributed all over the CMOS circuit area. The interface pins are of two types (providing contacts to the lower and higher levels of nanowiring); pins of each type are located on a square lattice of period $2\beta F_{CMOL}$ that is inclined by a small angle $\alpha = \arcsin(F_{nano}/\beta F_{CMOL}) \ll 1$ relative to the nanowire arrays. This trick allows an individual access to each nanowire crosspoint even if the ratio $F_{nano}/\beta F_{CMOL}$ is very small. For example, if the CMOS system applies, via the pin shown in blue in Fig. 1b, voltage V_h to the corresponding quasi-horizontal nanowire, and voltage $-V_v$ (through red pin 2) to the corresponding quasi-vertical nanowire, then the left nanodevice (of the only two shown in this picture) will be biased with larger voltage ($V_h + V_v$) than any other device. For nonlinear devices with a sharp threshold voltage V_t (within the range $V_h, V_v < V_t < V_t + V_v$), such selection allows the activation of a single device of the whole array. By moving the bias $-V_v$ from pin 2 to, *e.g.*, pin 2' (Fig. 1b) we may alternatively select the right nanodevice. Note that the distance between the individually selected nanodevices may be as small as $2F_{nano}$, *i.e.*, much less that the CMOS wiring pitch $2F_{CMOS}$.

The CMOL approach may enable, in future, an unprecedented density of useful devices. The only fundamental physical limitation here is the direct quantum tunneling between the nanowires; it limits the half-pitch F_{nano} at the level of the order of 3 nm and hence the nanodevice density at approximately 10^{12} cm^{-2}. Moreover, since the density of CMOS devices may be much lower than that number, the total fabrication costs of CMOL chips may be quite acceptable.

Recently, we have analyzed[16,19-22] several possible applications of CMOL circuits. The main requirement to the architectures of such circuits and systems is high defect tolerance, because it is hard to expect that even in the future the molecular self-assembly yield would ever reach 100%. This tolerance may be most simply implemented in embedded memories and stand-alone memory chips, with their simple matrix structure. In such memories, each molecular
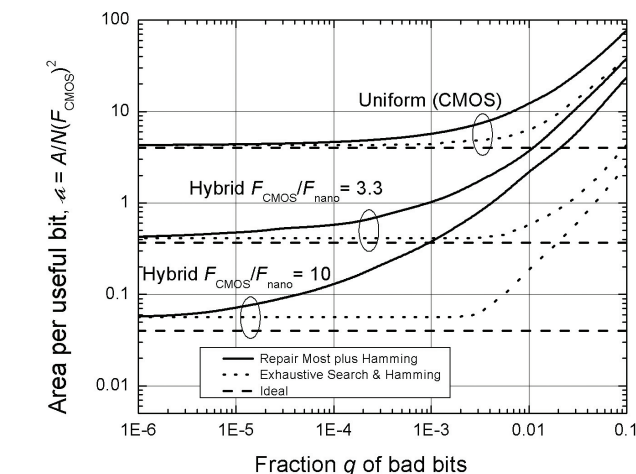

FIG. 2. *The area per useful bit after the memory optimization, as a function of single bit yield, for hybrid and purely semiconductor memories, in each case for two defect tolerance increase techniques.*
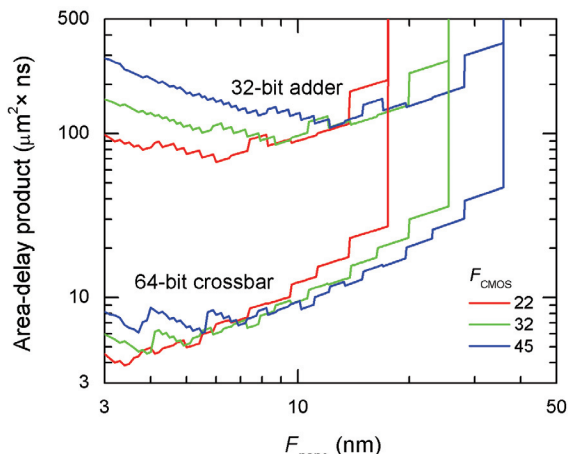

FIG. 3. *Calculated delay-area product of two simple digital circuits implemented in CMOL FPGA, as a function of nanowire half-pitch F_{nano}, for several values of CMOS subsystem half-pitch F_{CMOS}, at the corresponding values of power dissipation.[4]*

device (for example the single-electron latching switch[16]) plays the role of a single-bit memory cell, while the CMOS subsystem is used for coding, decoding, line driving, sensing, and input/output functions. Figure 2 presents the bottom line of our analysis of such memories[19]: the optimized area per bit as a function of the molecular device yield, for two values of the F_{CMOS}/F_{nano} ratio and two defect tolerance improvement techniques. (Results for purely CMOS memories are also shown for comparison.) The results indicate that CMOL memories with F_{CMOS} as moderate as 32 nm may reach density up to ~300 Gb/cm^2, i.e. enable terabit integration. However, for realistic algorithms of bad bit exclusion and error correction, the defect tolerance is not too high. For example, in a realistic case $F_{CMOS}/F_{nano} = 10$, for the simple and fast repair, most algorithm

combined with Hamming-code error correction, the bad bit fraction cannot exceed ~0.1% for a 90% chip yield.

In very recent work[20] we have shown that, somewhat counter-intuitively, higher defect tolerance, at very high performance, can be reached in reconfigurable CMOL FPGA-type logic circuits. For example, an integer 32-bit Kogge-Stone adder implemented using such arrays may feature ~20% defect tolerance for yield above 99%, simultaneously providing the performance (in terms of the area-delay product) about 500 times higher than a purely semiconductor-transistor FPGA using the same CMOS technology, at acceptable power dissipation (Fig. 3).
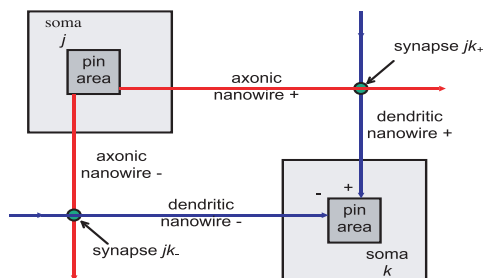
Future Directions

Fig. 4. The general structure of a CMOL CrossNet (for the simplest case of a non-Hebbian, feed forward network). Within the simplest "Fire Rate" approach, neural cell bodies ("somas") are just differential anlog ampifir.

Finally, very optimistic results have been also obtained[21,22] for one more prospective application of CMOL circuits, mixed-signal neuromorphic networks with the special Distributed CrossBar Network ("CrossNet") architecture (Fig. 4). In such a network, neural cell bodies ("somas"), that are relatively sparse, are implemented as analog CMOS amplifiers, nanowires are used as axonic and dendritic connections, while the molecular latching switches serve as elementary binary-weight synapses that control coupling between the neural cells. We have demonstrated[21,22] that despite the restrictions imposed by this hardware implementation, CMOL CrossNets can be "trained" to perform essentially any function demonstrated with software-implemented neural networks, including image recognition and pattern classification. This result is very significant, because CMOL circuits may operate much faster, and with much larger input data vectors, than the neural network programs run on usual computers. Moreover, estimates show that CMOL CrossNet chips may have a real density higher than biological networks (say, the human cerebral cortex), at much higher speed, at manageable power dissipation. These estimates give an additional motivation for the further development of CMOL CrossNet circuits.

The development of CMOL technology (especially the high-yield molecular self-assembly) will certainly require a major industrial effort and substantial time period, probably not less than 10 to 15 years. However, this timing may be still acceptable to prevent the impending crisis of Moore's law, provided that we start right now. ∎

References

1. V. A. Sverdlov, T. J. Walls, and K. K. Likharev, *IEEE Trans. Electron Devices*, **50**, 1926, (2003).

2. Semiconductor Industry Association, *International Technology Roadmap for Semiconductors, 2004 Edition*, http://public.itrs.net.

3. K. K. Likharev, *IEEE Proc.*, **87**, 606 (1999).

4. K. K. Likharev, in *Nano and Giga Challenges in Microelectronics*, J. Greer *et al.*, Editors, p. 27, Elsevier, Amsterdam (2003).

5. J. H. Fendler, *Chem. Mater.*, **13**, 3196 (2001).

6. J. Tour, *Molecular Electronics*, World Scientific, Singapore (2003).

7. H. Park, *et al.*, *Nature*, **407**, 57 (2000).

8. S. P. Gubin, *et al.*, *Nanotechnology*, **13**, 185 (2002).

9. N. B. Zhitenev, H. Meng, and Z. Bao, *Phys. Rev. Lett.*, **88**, 226801 (2002).

10. J. Park, *et al.*, *Nature*, **417**, 722 (2002).

11. S. Kubatkin, *et al.*, *Nature*, **425**, 698 (2003).

12. M. R. Stan, *et al.*, *IEEE Proc.*, **91**, 1940 (2003).

13. Y. Chen, *et al.*, *Nanotechnology*, **14**, 462 (2003).

14. Z. H. Zhong, *et al.*, *Science*, **302**, 1377 (2003).

15. C. Li, *et al.*, *Appl. Phys. Lett.*, **84**, 1949, (2004).

16. K. K. Likharev and D. B. Strukov, accepted for publication in *Introducing Molecular Electronics*, G. Cuniberti, *et al.*, Editors, Springer, Berlin (2005); preprint available online at http://rsfq1.physics.sunysb.edu/~likharev/nano/Springer04.pdf.

17. S. Zankovych, *et al.*, *Nanotechnology*, **12**, 91 (2001).

18. S. R. J. Brueck, *et al.,* in *International Trends in Optics*, A. Guenther, Editor, p. 85, SPIE Press, Bellingham, WA (2002).

19. D. B. Strukov and K. K. Likharev, *Nanotechnology*, **16**, 137 (2005).

20. D. B. Strukov and K. K. Likharev, "CMOL FPGA: A reconfigurable architecture for hybrid digital circuits with two-terminal nanodevices", Submitted for publication in *Nanotechnology*; preprint available online at http://rsfq1.physics.sunysb.edu/~likharev/nano/FPGA05.pdf.

21. Ö Türel and K. K. Likharev, *Int. J. Circ. Theor. Appl.*, **31**, 37, (2003).

22. Ö. Türel, J. H. Lee, X. Ma, and K. K. Likharev, *Int. J. Circ. Theor. Appl.*, **32**, 277 (2004).

About the Author

Konstantin K. Likharev is a Distinguished Professor of Physics in Stony Brook University (State University of New York). The main current focus of his research group is nanoelectronics: http://rsfq1.physics.sunysb.edu/~likharev/nano/. He can be reached at klikharev@notes.cc.sunysb.edu.

Future Directions