Semiconductor Cleaning Technology: Forty Years in the Making

by Jerzy Ruzyllo

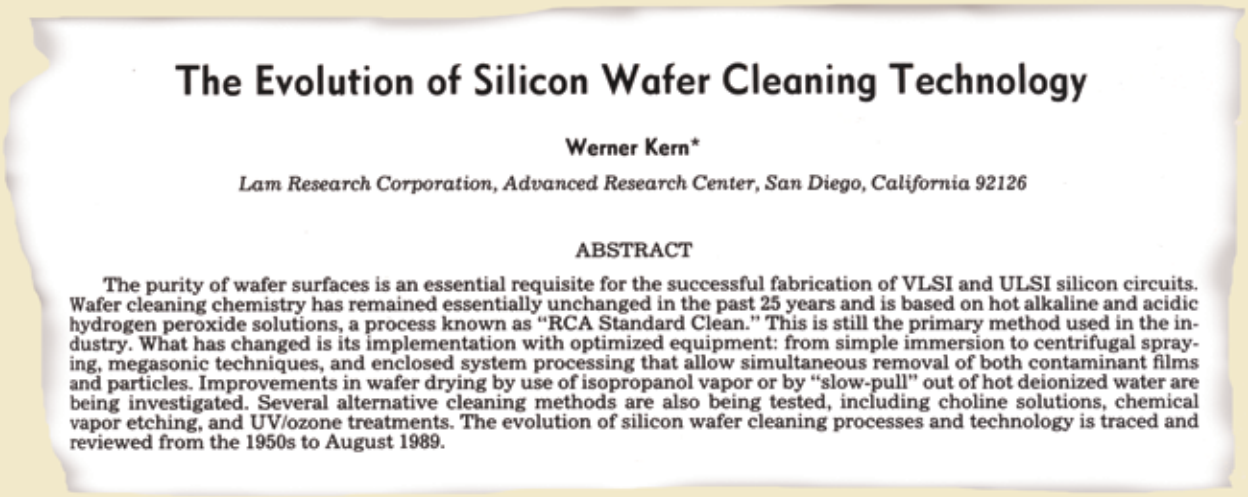
Wafer cleaning operations employed in semiconductor device manufacturing do not serve the purpose of building device features by adding films, or defining geometries, by altering conductivity of semiconductors, or forming contacts and interconnects. In addition to not serving any of these purposes, wafer cleaning consumes significant amounts of resources, and demands waste disposal, making it a very costly operation. Yet, in spite of all this, it is the most frequently applied operation in a typical semiconductor device manufacturing sequence; and is an operation that plays a pivotal role in determining manufacturing yield. While the exact numbers in this regard are not available in the public domain, it can be safely assumed that in advanced integrated circuit (IC) manufacturing at least one third of all operations performed on the wafer are cleaning operations. Its role in the overall sequence and impact on the manufacturing yield was growing as device geometries were getting tighter and the quality of silicon wafers was improving, thus, reducing an adverse impact of bulk defects.

Considering the importance of wafer cleaning in semiconductor manufacturing it comes as no surprise that related papers, devoted to silicon cleaning in particular, are very common in technical literature, with ECS publications being no exception. The Electronics and Photonics Division (EPD) of the Society early on recognized the importance of cleaning as a self-contained scientific and technical domain by starting a series of topical symposia devoted to cleaning technology in semiconductor device manufacturing twenty years ago. Some seven hundred papers devoted to cleaning technology were published in the materials from the eleven symposia in this series.[1]

The First International Symposium on Cleaning and Surface Conditioning Technology in Semiconductor Device Manufacturing was held in 1989. It was the very first topical symposium devoted entirely to the problems of surface cleaning and contamination control in semiconductor manufacturing. The highlight of the meeting, and its keynote presentation, was an invited talk delivered by Werner Kern entitled "The Evolution of Silicon Wafer Cleaning Technology."[2] The same paper, subsequently published in the *Journal of The Electrochemical Society*[3] has become the 51st most-cited paper published in the society's *Journal* to date. In this paper, Kern traces and discusses the evolution of silicon wafer cleaning over a time spanning 40 years, starting in early 1950s. An interesting part of the discussion involves a description of the very early silicon cleaning efforts in which quite often "cleaning" operations were inflicting more damage to the wafer than improving the quality of its surface. For instance, the use of mixtures of sulfuric acid-chromic acid led to chromium contamination of the wafer and caused ecological problems when disposing of it.

Werner Kern was uniquely qualified to present an overview of silicon cleaning evolution because it was he who, with his colleague D. Puotinen, was responsible for a real breakthrough in semiconductor cleaning technology. In their seminal paper entitled "Cleaning Solution Based on Hydrogen Peroxide for Use in Semiconductor Technology" published in 1970[4] Kern and his partner proposed the very first systematically developed silicon cleaning processes based on a two-step oxidizing and complexing treatment with hydrogen peroxide solutions: (1) an alkaline mixture at high pH followed by (2) an acid mixture at low pH. Called an "RCA clean," and alternatively referred to as a "standard

FROM:
W. Kern, "The Evolution of Silicon-Wafer Cleaning Technology," *J. Electrochem. Soc.*, **137**, 1887 (1990).



The Evolution of Silicon Wafer Cleaning Technology

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ABSTRACT

The purity of wafer surfaces is an essential requisite for the successful fabrication of VLSI and ULSI silicon circuits. Wafer cleaning chemistry has remained essentially unchanged in the past 25 years and is based on hot alkaline and acidic hydrogen peroxide solutions, a process known as "RCA Standard Clean." This is still the primary method used in the industry. What has changed is its implementation with optimized equipment: from simple immersion to centrifugal spraying, megasonic techniques, and enclosed system processing that allow simultaneous removal of both contaminant films and particles. Improvements in wafer drying by use of isopropanol vapor or by "slow-pull" out of hot deionized water are being investigated. Several alternative cleaning methods are also being tested, including choline solutions, chemical vapor etching, and UV/ozone treatments. The evolution of silicon wafer cleaning processes and technology is traced and reviewed from the 1950s to August 1989.

clean," or SC, the process has set the ground rules for Si cleaning which are valid until today. Originally focused primarily on the removal of the organic surface films and metallic contaminants, the process, and specifically its first "alkaline component," was proven to be very effective in the removal of the particulate contaminants from the Si surface as well. Called RCA1, or SC1, or AHP (Ammonia-Hydrogen Peroxide) it remains until today a cornerstone of any Si cleaning sequence. Very broadly employed, this process makes the impact of the paper in which it was proposed[4] to be beyond any measure. The author was not able to determine the number of citations, but there is no doubt this paper is among the most frequently cited of all in semiconductor related literature.

Kern's contribution to silicon cleaning science and technology came not only in the form of the above mentioned papers. He was also an editor and lead contributor to the first monograph devoted entirely to semiconductor cleaning[5] as well as an organizer and the lead instructor in the series of the very first short courses devoted to silicon cleaning technology organized in 1991-1993. Considering all these contributions, the impact Werner Kern had on the birth and subsequent evolution of silicon cleaning science and technology cannot be overestimated.

The visibility and impact of semiconductor cleaning in ECS publications is not limited to seminal contributions by Werner Kern. It is further underscored by the presence of yet another cleaning-devoted paper on the list of top 100 most cited papers from the *Journal of The Electrochemical Society*. In fact, the most frequently cited paper published in the *Journal* (1,000+ citations) is the silicon cleaning related paper by A. Ishizaka and Y. Shiraki entitled, "Low Temperature Surface Cleaning of Silicon and Its Application to Silicon MBE."[6] Interestingly, this paper was not devoted to the mainstream wet cleaning technology but instead it proposed a hybrid cleaning approach for Si molecular beam epitaxy (MBE). In the proposed process the more or less conventional wet cleaning sequence, including RCA1 and RCA2 steps, was followed *in situ* inside the MBE chamber by relatively low-temperature (710°C) thermal cleaning carried out in ultra-high vacuum of 2 x 10^{-11} torr. The result was a carbon and oxygen-free Si surface prior to Si epitaxial growth (see Fig. 1). The concept of oxide removal from the Si surface in high vacuum at high temperature was not new, see Ref. 7. Ishizaka and Shiraki are credited for developing it into the much lower-temperature, manufacturing-ready process which leaves silicon surface prior to MBE growth pristinely clean.

The spectacular success, in terms of the number of citations, of this paper was related not only to its technical value, but also to the timeliness of the proposed approach. With the rapid improvements in vacuum technology in the early 1980s the growth of molecular beam epitaxy that followed did offer viable solutions to the problems mainstream silicon technology was expected to face in the future. With time, this promise was amply fulfilled as the MBE was instrumental in the introduction of strained channel technology into the mainstream cutting edge silicon CMOS manufacturing. It is unfortunate that the approach proposed by Ishizaka and Shiraki requires an ultra-high vacuum, which is inherent to the MBE process, as well as application for the period of time of the relatively high temperature. Because of it, it cannot be extended to the other processes that require stripping of the native oxide from the silicon surface such as pre-contact metallization surface treatments.

From this author's perspective, an interesting aspect of Ishizaki and Shiraki's contribution was that it was among the very early *Journal of The Electrochemical Society* publications in which a complete silicon cleaning sequence incorporating a "dry" surface treatment component was proposed. In fact, the Society's *Journal* was a preferred venue for several other early reports on the investigations of various silicon dry cleaning procedures (*e.g.* Refs. 8 and 9). It was also in the *Journal of The Electrochemical Society* where one of the very first complete and fully functional entirely gas-phase pre-gate oxidation cleaning procedures was proposed.[10]

There is no doubt that the above discussed two major contributions, each in its own way, had an impact on several important developments in semiconductor cleaning science and technology. For over 40 years, this technical and scientific domain continues to grow both in terms of knowledge base, as well as tool engineering. Unfortunately, challenges are growing as well. For instance, particles to be controlled now are two orders of magnitude smaller than two decades ago and metallic contaminants must be controlled at a two orders of magnitude lower level. The good news, however, is an overall reduction of contamination in the advanced semiconductor manufacturing environment. Without

FROM:
A. Ishizaka and Y. Shiraki, "Low Temperature Surface Cleaning of Silicon and Its Application to Silicon MBE," *J. Electrochem. Soc.*, **133**, 666 (1986).

Low Temperature Surface Cleaning of Silicon and Its Application to Silicon MBE

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ABSTRACT

A low temperature thermal cleaning method for Si molecular beam epitaxy (MBE) is proposed. This method consists of wet chemical treatment to eliminate carbon contaminants on Si substrates, thin oxide film formation to protect the clean Si surface from contamination during processing before MBE growth, and desorption of the thin oxide film under UHV. The passivative oxide can be removed at temperatures below 800°C. It is confirmed that Si epitaxial growth can take place on substrates cleaned by this method and that high quality Si layers with dislocations of fewer than 100/cm² and high mobility comparable to good bulk materials are formed. Surface cleanliness, the nature of thin passivative oxide films, and cleaning processes are also studied by using such surface analytic methods as Auger electron spectroscopy, reflection high energy electron diffraction, and x-ray photoelectron spectroscopy.

significantly reduced particle counts in process ambient, much cleaner chemicals and photoresist, as well as cleaner and more efficient wafer storage and handling, the progress in cleaning technology alone would not be able to support the growth of semiconductor industry which was taking place.

In the evolution of cleaning technology based on ideas introduced by the papers discussed in this overview, selected trends can be readily distinguished.[11] Wet cleaning remains to be the "work horse" of state-of-the-art wafer cleaning, although, an extreme mechanical fragility of nano-features as well as a range of new materials presently used to build an advanced integrated circuit will force increased emphasis on dry cleaning technology. While present wet cleaning chemistries did not depart far from the original RCA recipes, the use of heavily diluted solutions, focus on process simplification, emphasis on single wafer cleaning, and a broad use of ozonated water are typical for today's cleaning sequences. Furthermore, the emergence of new materials such as low- and high-k dielectrics, along with metal gates and copper, all make state-of-the-art wafer cleaning technologies differ significantly from those used in the past.

Selectivity of cleaning is an issue which was not a key factor in the past. The growing challenge is to remove contaminants from the wafer surface without attacking, or altering properties of materials that are exposed to cleaning chemistries. For instance, dielectric constant of highly sensitive porous low-k interlayer dielectrics may increase significantly as a result of interactions with liquid chemistries. As a result, various alternative non-aqueous techniques such as supercritical CO_2 (SCCO2) cleaning, cryogenic nitrogen aerosol cleaning, low-pressure, increased temperature HF vapor cleaning, among others, are either already used in mainstream manufacturing, or are expected to be used in the near future. One of the most obvious facets of this transition is a need to differentiate between FEOL and BEOL cleaning methods with focus on post-CMP cleans in the latter case. The maturity of point-of-use chemical generation, as well as strong emphasis on recycling and more efficient waste disposal, should also be stressed in this context.

The concluding observation from this review is that wafer cleaning technology, of which two papers considered here are true cornerstones, is keeping up with increasing needs through continuous progress in all its facets. This progress will need to continue if the challenges resulting from increased complexity of device structures, new materials used, and the need to address environmental concerns are to be resolved. If past developments are any indication, however, with the type of leadership provided by the two so-highly cited papers discussed above, semiconductor cleaning science and engineering is very likely to respond successfully to any future challenge.

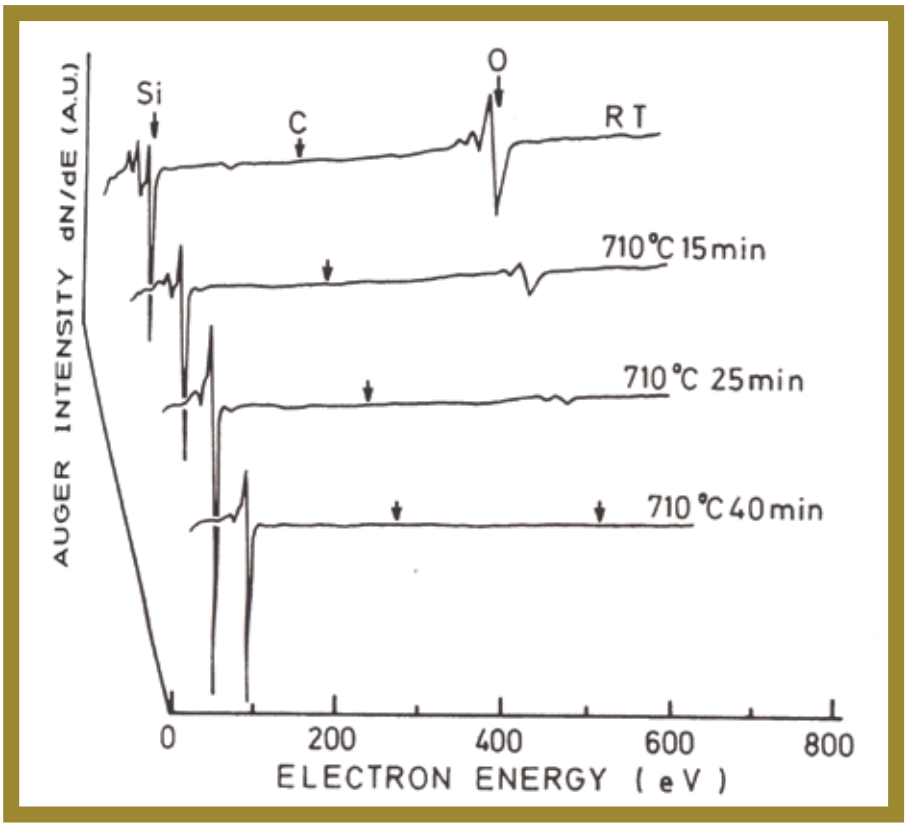

Fig. 1. In situ *Auger spectra of Si surfaces after iso-thermal heating at 710°C (From Ref. 6).*

About the Author

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