Hot Topics in Electrodeposition

*The hard work of three leading researchers was recently interrupted when I asked them to ponder the following question: "What, in your view, is an exciting, major development in electrodeposition over the last five years?" Believe it or not, they each had a different answer! Many thanks to Andy Gewirth, Panos Andricacos, and Jay Switzer for sharing their perspectives. —***jd**

by Andrew A. Gewirth, Panos C. Andricacos, and Jay A. Switzer, with John O. Dukovic, editor

Scanning-Probe Microscopes in Electrodeposition

by Andrew A. Gewirth

One of the most exciting developments in electrodeposition over the last five years has been the use of scanning probe microscopes (SPM) to study, characterize, and affect this process. Electrodeposition creates metallic and semiconductor deposits with surfaces of varying properties and structure. SPM is exquisitely sensitive to the structure of surfaces at many levels. For years, studies of electrodeposition involved the analysis of electrochemical transients coupled with visual, spectroscopic, or electron microscopic analysis. From these somewhat indirect measurements, the growth and structure of the deposit were inferred. With the invention of scanning probe microscopes and their subsequent use to study electrochemical processes (1), textures and growth processes once only inferred are now directly visualized. As recently as five years ago, SPMs were only beginning to be used to study electrochemical processes. Now SPMs are ubiquitous in electrochemical laboratories — and no more so than in laboratories where electrodeposition is studied.

The advantages of using SPM to study electrodeposits are many. First, SPMs provide very accurate information about the topology of the deposit. This topology or height function is an important component of any subsequent modeling of the growth of the surface. The detail available from SPMs is evident in the series of images shown in FIG. 1 (2). The images show the evolving structure of a Cu electrodeposit on a gold surface in a plating bath containing trace amounts of an organic additive. The images show that in this particular case, growth starts at step edges and grows onto the terraces of the substrate.

The second advantage of SPM is that the measurement can be performed with the growing electrodeposit still in solution. This eliminates problems with oxide or other interfering species that may form on the surface following emersion from solution. Third, the SPM can obtain atomic resolution so detailed structures on the surface can be seen. This has allowed workers in the area to examine the texture of the deposit with high resolution to see hitherto unresolved detail. An example here would be the recent observation of the growth of linear monolayer Ni deposits on Au(111) (3).

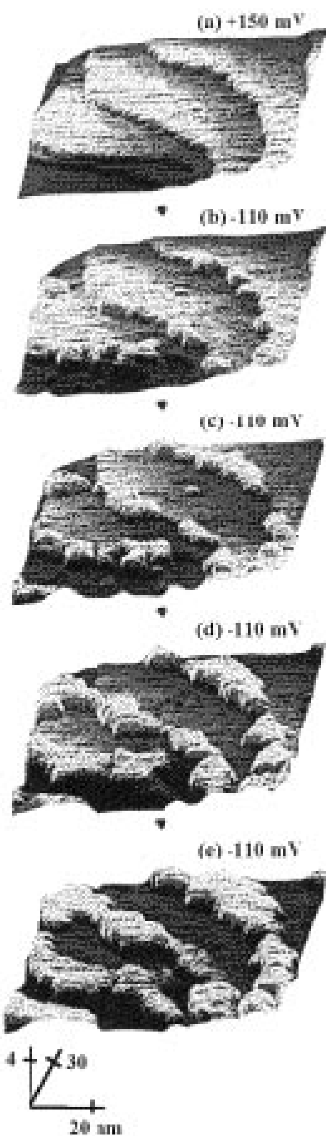

FIG. 1. In-situ STM images taken before (a) and during (b) - (e) bulk copper deposition onto a gold film in 0.1 M H_2SO_4 + 50 μM$CuSO_4$ + 25 μM crystal violet. The copper deposit decorates the step edges.

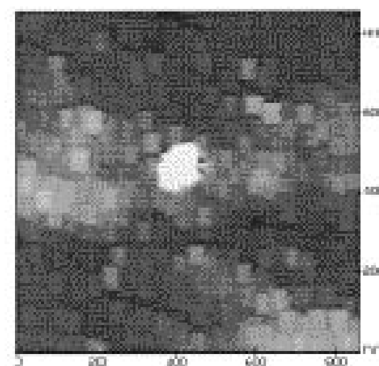

FIG. 2. In-situ AFM image of a Cu(110) surface in a $HClO_4$ solution (pH=2.45) showing a single 60-nm-high feature formed by enhanced deposition of Cu onto the surface following high-force scanning in the central area during Cu deposition.

Finally, the probe microscopies can actually manipulate surface structures. FIGURE 2 shows a result from our group using an AFM tip to remove passivating agents in a particular location and nucleate Cu growth at that site (4). There have also been a large number of examples of small structure fabrication using SPM (5). The hope is to fabricate uniquely small features which may be useful as sensors, in electronic applications, or as catalysts.

The ability to visualize the electrodeposit growth process and to examine with high resolution the effects of additives and other parameters makes possible an efficient feedback mechanism. This mechanism is important not only for understanding what present electrodeposition technology can do, but also for designing new technology for the future. ■

Electroplated Copper Wiring on IC Chips

by Panos C. Andricacos

Heralded as a "major breakthrough" in *The New York Times* (Sep. 22, 1997) and a "dazzling technical advance" by *Time* magazine (Oct. 10, 1997), the change from aluminum to copper in semiconductor interconnect technology is promising to deliver better and cheaper chips and, in the long run, permeate the entire semiconductor industry. And electroplating has a good chance of being the preferred method for depositing copper, as indicated in reports from several sources, making this perhaps one of the most significant events in electrodeposition technology in recent years (6,7).

Use of copper as the interconnect conductor enables a decrease in the number of metal layers needed for the optimal operation of chips, especially if combined with an insulator that has a lower dielectric constant than silicon dioxide used presently. Because of its superior resistance to electromigration, copper wiring permits higher current densities without failure and therefore higher reliability. Finally, "Dual-Damascene processing" makes it possible to fabricate a via and a line level simultaneously; this and the aforementioned advantages of copper lead not only to superior chip performance, but also to potentially lower-cost manufacturing processes (8).

Dual-Damascene processing and the overriding need of a barrier (FIG. 3) to prevent copper from contaminating the insulator as well as reaching the underlying semiconductor devices (6,9,10) confront the electrochemist—as well as anyone attempting to deposit the copper metal—with the difficult task of providing a completely filled structure, one in which voids (and possibly subsequent entrapment of electrolyte) are completely absent. We have found that of all the methods of copper deposition, which include physical and chemical vapor deposition as well as electroless and electrolytic plating, the last appears to have produced consistently (6,10,11) the best results (FIG. 4) and is well on its way to being a process of great significance in semiconductor manufacturing. Damascene plating constitutes a radical deviation from the more traditional plating-through-mask technology that has been used in the manufacture of disk drives and other computer components, and places emphasis on aspects of plating technology (such as microthrowing power) that have never before received the scrutiny of a semiconductor manufacturing environment.

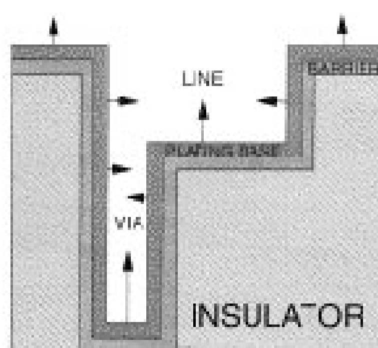

FIG. 3. Schematic depiction of a dual Damascene structure immediately prior to copper electroplating; arrows indicate direction of growth of the plated copper.

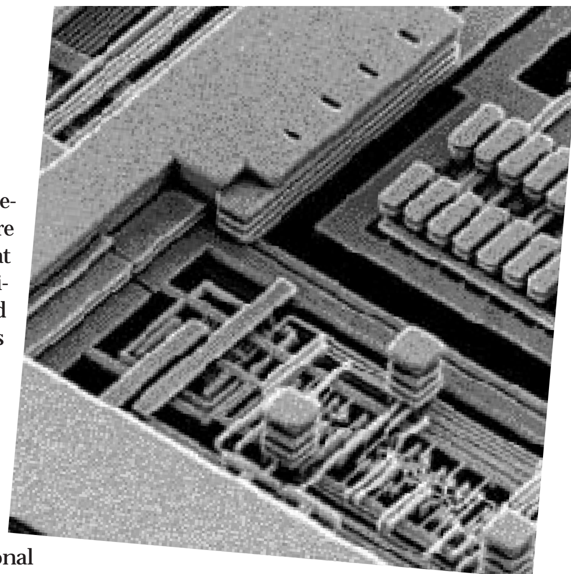

FIG. 4. SEM view of IBM's first-to-market six level copper interconnect technology (courtesy of IBM Microelectronics, http://www.chips.ibm.com/sa27/images/iso7.jpg).

It is only a matter of speculation what kinds of changes the implementation of copper plating in the semiconductor industry will cause to the infrastructure of the plating industry as well as to the understanding of the field itself. Plating is considered by many to be more of an art than a science; people experience a shock when they see precious wafers being immersed in blue liquids many times during the fabrication process. But when these wafers perform better than others, all prejudice goes away and yields its place to enthusiasm for something new and useful.

The Electrochemical Society is responding to the emerging significance of electroplating in interconnection technology, and a conference entitled "Electrochemical Processing in ULSI Fabrication I" is being organized for the 1998 San Diego meeting. There is no doubt that this new application of electrochemistry will be the subject of much valuable research and many interesting discussions at this conference and in the future. ■

Electrodeposition of Nanoscale and Nanophase Materials

Jay A. Switzer

Electrodeposition is a pretty cool technique. At the relatively low temperatures of electrodeposition (often room temperature), interdiffusion is not much of a problem, and nanoscale and nanophase materials can be electrodeposited. Notice the use of the word "material" instead of "metal." Many different types of materials (metals, ceramics, semiconductors, conducting polymers, superconductors, etc.) can be produced electrochemically. It is also significant that these materials can be electrodeposited on a nanometer scale.

What is the big deal about small structures? As the size of materials approach molecular dimensions, quantum effects become important. In the nanometer-size regime, the properties of a material (optical, electrical, magnetic, chemical, and mechanical) become a function of size. The experimenter can tune the properties of the material by simply dialing-in a desired size. In addition to having materials with small dimensions, it is also important that the distribution of sizes is tight, and it is usually preferred that the nanostructures are ordered in some way.

George Attard and co-workers at the University of Southampton have very recently shown that mesoporous platinum films can be electrodeposited from liquid crystalline plating solutions (12). The pores form an ordered hexagonal array on the electrode surface. In these films, the diameters of the holes (1.7 to 10 nm) are determined by the length of the alkyl chain of the surfactant, and the geometric disposition of the channels is determined by the architecture of the liquid crystalline phase. The volumetric capacitance, estimated to be about 200 F/cm^3, is typical of the best candidates for electrochemical capacitors.

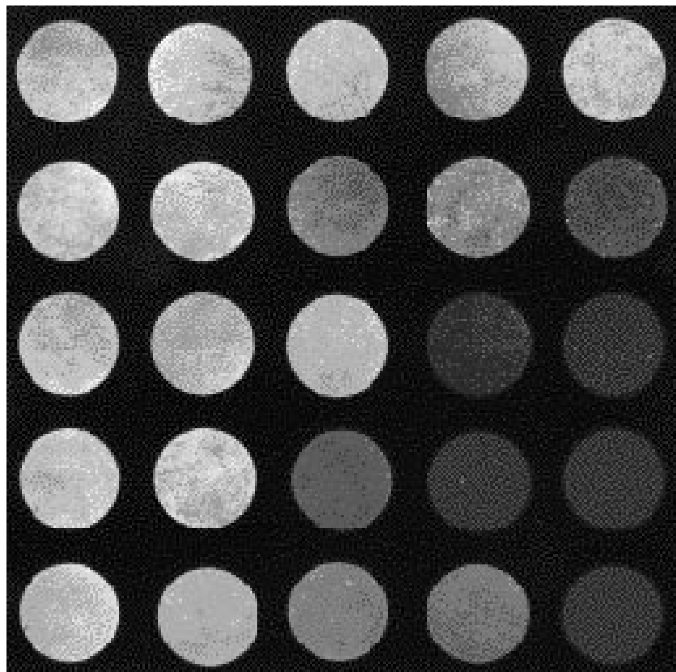

FIG. 5. Photomicrographs of 25 samples of the alumina membranes (each 6 mm in diameter) after the deposition of gold fibrils of various aspect ratios into membranes with pores of various diameters.

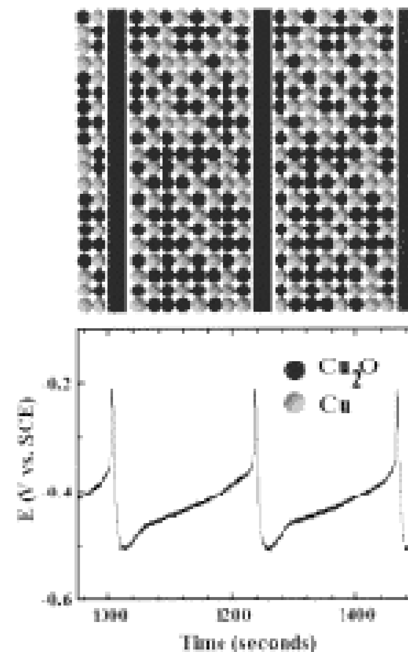

FIG. 6. Schematic of a self-assembled copper/ cuprous oxide layered nanostructure (top), and the potential oscillations that are observed during constant-current deposition of the nanostructure (bottom). The cuprous oxide layer is 3 nm thick.

An approach pioneered by Chuck Martin's research group at Colorado State University entails the electrodeposition of metals, semiconductors, oxides, or conductive polymers within the pores of nanoporous template membranes (13). This group has prepared ensembles of nanofibers or nanotubules of materials that protrude from the electrode like the bristles of a brush. FIGURE 5 shows beautifully colored films of gold nanofibrils in alumina pores that have been grown by this group (13). The tunable colors resulted from the plasmon resonance band of the metal (like the well-known size-dependent color of gold colloids). They have also produced metal nanotubule membranes that show electrochemically switchable ion-transport selectivity (14).

Reg Penner's group at the University of California - Irvine has developed a hybrid electrochemical/chemical (E/C) method to synthesize epitaxially-oriented nanocrystallites on graphite surfaces. They have used this method to deposit quantum dots of CdS and CuI (15,16). In the E/C deposition of CdS, cadmium metal nanocrystals are first electrochemically deposited onto the graphite basal plane surface. The Cd is then oxidized at high pH to $Cd(OH)_2$, followed by immersion in an aqueous sulfide solution to produce wurtzite CdS. Nanocrystallites of CdS located within the boundaries of a single grain on the graphite possess identical azimuthal orientations. In a wonderful example of bandgap engineering, the Penner group showed that they could blue-shift the luminescence of CuI quantum dots from the weak to strong confinement limit by systematically decreasing the size of the dots.

Gary Hodes and Israel Rubinstein of the Weizmann Institute in Israel have shown that CdSe quantum dots in the 5 nm range can be epitaxially electrodeposited directly from nonaqueous solution onto evaporated Au(111) films (17). They showed that the size of the quantum dots was controlled by the strain induced by the lattice mismatch (18). Using a modified scanning force microscope they showed evidence of single-electron Coulomb charging of the quantum dots (19).

The Switzer group's approach to the nanoregime has been to produce nanometer-scale multilayers and superlattices electrochemically. We have previously produced both defect-chemistry and compositional superlattices based on conducting metal oxides (20,21). These superlattices were produced by pulsing either the applied current or potential during deposition. In a new twist on this work, we have very recently found that layered nanostructures of copper metal and cuprous oxide (a p-type semiconductor) self assemble during galvanostatic deposition (22,23). The electrode potential spontaneously oscillates during constant-current electrodeposition. FIGURE 6 shows representative potential oscillations, and a cartoon of the proposed Cu/Cu_2O layered nanostructure. We are very interested in the electrical properties of these layered materials, since the cuprous oxide layers are of tunneling dimensions.

These are a few examples of the work on the electrodeposition of nanophase materials that is being done in the world. A variety of tricks can be used to prepare these "designer solids" with narrow size distributions and ordered nanostructures. The electrochemical method is cheap, relatively simple, and it can often produce nanostructures that cannot be made by other methods. To learn more about this research area, attend symposium M2 on "Electrodeposition of Nanoscale and Nanophase Materials" at the 194th meeting of The Electrochemical Society in November, 1998 in Boston. ■

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About the Authors

Andrew A. Gewirth is a professor of chemistry at the University of Illinois at Urbana-Champaign.

Panos C. Andricacos is manager of Electrodeposition Technology at IBM's T. J. Watson Research Center in Yorktown Heights, New York.

Jay A. Switzer is Curators' Professor in the Department of Chemistry and Senior Investigator in the Materials Research Center at the University of Missouri-Rolla.

John O. Dukovic (chair of the ECS Electrodeposition Division) is a research staff member and project leader at IBM's T. J. Watson Research Center in Yorktown Heights, New York.