Silicon Materials Science and Technology VIII

The history and future of integrated circuit performance takes center stage

by Howard R. Huff

The International Symposia on Silicon Materials Science and Technology, sponsored by the Electronics Division, has provided a unique historical record of the progress in our understanding of silicon materials over the last 30 years. A common thread throughout the series has been the characterization, annihilation, and, in some cases, the selective utilization of defects to achieve superior integrated circuit (IC) performance, reliability, and yield. Since many of the phenomena discussed are structure-sensitive, the "process-structure-property" approach has been adopted wherein the fabrication process determines the structure, which thereby determines the material properties. This approach continues to be critical to the fabrication and interpretation of IC product characteristics, including correlation with in-process monitors and process/device/IC models. The silicon symposium series has not only provided the forum for the global sharing of trends in silicon materials; it has also provided a platform to enhance communication between material scientists and device/IC personnel. The series, for example, has highlighted selective metal oxide semiconductor (MOS) device scaling by Bob Dennard and Alex Broers in 1973; physical limits in silicon microelectronics by Bob Keyes, SUPREM modeling by Bob Dutton et al., and IC process engineering models by Jim Meindl et al. in 1977; perspectives on very-large scale integration (VLSI) by Gordon Moore and the Japanese VLSI Cooperative Laboratories by Yasuo Tarui and Yoshiyuki Takeishi in 1981; ULSI interconnection limits by Jim Meindl in 1986; MOS transistor scaling by Al Tasch and Hyungsoon Shin, device and ICs for the computer age by Jun-ichi Nishizawa and dynamic random access memory (DRAM) cell structures for the ULSI era by Yoichi Akasaka in 1990; and ULSI trends by Eiji Takeda in 1994.

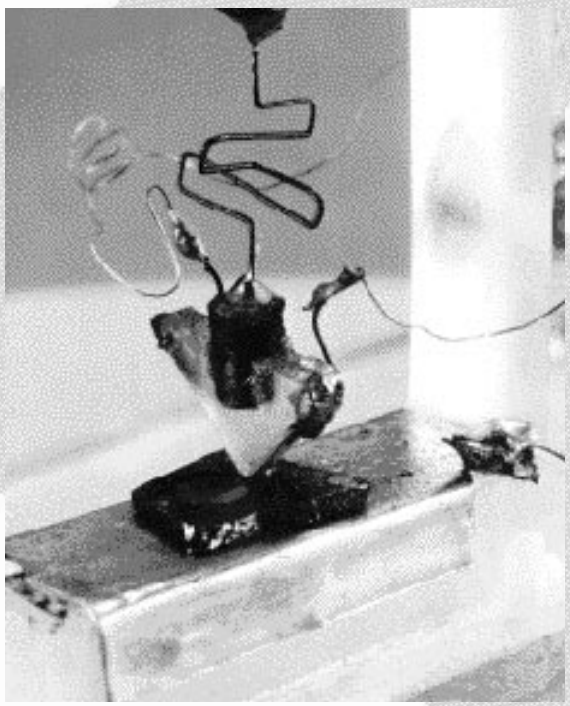

FIG. 1: Bardeen and Brattain's point-contact semiconductor amplifier. (Property of AT&T Archives. Reprinted with permission of AT&T.)

The 1998 Silicon Symposium in San Diego (co-chaired by the author, Ulrich Gösele of the Max Planck Institute, Germany and Hideki Tsuya of Sumitomo Sitix, Japan) is especially significant inasmuch as we are celebrating the 50th anniversary of the commercial introduction of the point-contact transistor (see FIG. 1). Accordingly, the historical roots of the microelectronics industry, as well as the anticipated directions for its future growth, will be discussed in a special historical session, *Fifty Years and Counting*, co-chaired by Hans Queisser and Jim Meindl. Eighteen scientific and engineering leaders who have significantly contributed to the microelectronics revolution will address the symposium during this session. These reviews, however, will represent more than the authors' perception of their contributions in an historical setting. The authors also will focus on the creative directions, the future scientific and engineering challenges, the opportunities envisioned for their field's growth, and how their field will impact ULSI as we approach the 21st century. The 18 papers are grouped into the three broad categories of Threshold Events, Materials Issues and IC Fabrication, and Materials Issues and Device/IC Performance.

Fifty Years and Counting Historical Session

Threshold events.—Hans Queisser will introduce the session briefly recounting *Materials Research in Early Silicon Valley.* Queisser notes that although point contact transistor action was initially observed in grains of polycrystalline germanium and, subsequently, in grains of polycrystalline silicon, the importance of single crystal material (immediately recognized by Gordon Teal) and the introduction of single-crystal silicon were to have profound implications. Dislocations, epitaxial stacking faults, residual metallic point defects, gettering, and generation/recombination phenomena and their effect on the electrical characteristics of devices were extensively studied in the late fifties and early sixties in the initial Silicon Valley company established by Bill Shockley. Although Shockley's company (of which Queisser was a member) was initially formed with Arnold Beckman's evident intent to fabricate and market diffused-base transistors, Shockley's interest rapidly shifted to the pnpn bistable silicon diode. Although the pnpn diode was not commercially viable and eventually became defunct, Shockley's company became the prototype Silicon Valley company and the progenitor of Silicon Valley's genealogy. Shockley's 1974 article on *The Invention of The Transistor - An Example of Creative-Failure Methodology,* (1) will be included to complement Queisser's overview.

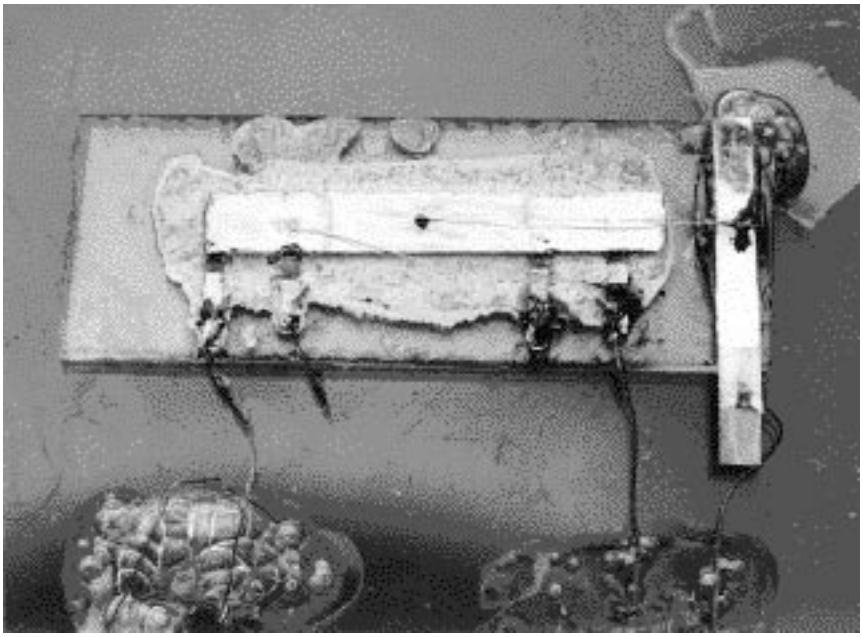

FIG. 2: The first integrated circuit, a phase-shift oscillator, invented by Jack S. Kilby of Texas Instruments in 1958. (Photograph courtesy of Texas Instruments.)

In his address, *The Four-Layer Diode in the Cradle of Silicon Valley*, Kurt Hubner (also a member of Shockley's company) further explores why, with the availability of junction transistor technology, Shockley chose to focus his company on the four-layer pnpn silicon diode. Hubner will discuss the importance of flaws in the space charge layer of silicon, which were critical in facilitating pnpn device functionality, why silicon was required, how the device was fabricated, and why it failed in the marketplace. Fred Seitz, currently President Emeritus of Rockefeller University, and Norman G. Einspruch, Professor at the University of Miami and former Director of the Central Research Laboratories at Texas Instruments, then will review *The Tangled History of Silicon in Electronics*. While silicon was the leading crystal rectifier in the pre-radio days of wireless communications, it was eclipsed for about 15 years as a result of advances in the development of triode vacuum tube technology. As a result of the unique role of silicon rectifiers in microwave research and then as a heterodyne mixer in radar, the requisite purification technologies implemented for silicon by Dupont and several other organizations will be reviewed. The special attention both silicon and germanium received during World War II, which made them attractive candidates for continued research at Purdue, General Electric and the University of Pennsylvania, etc., and the search for a solid-state semiconductor triode after 1945 at Bell Laboratories, will all be reviewed.

Diethard Huber of Wacker Siltronic will continue the discussion on the synthesis of polysilicon in Europe and its purification at the Siemens Pretzfeld Laboratories, which resulted in the Siemens polysilicon process, and facilitated the fabrication of high-power devices with the requisite high-resistivity and high-carrier lifetime. The development of trichlorosilane and float-zone technologies by Wacker Chemie Corporation for the mass production of devices will then be reviewed. Makoto Kikuchi of Tokai University (retired from SONY Corporation) will review Japanese work in the early days after World War II. The availability of silicon, which did not exhibit the amplification phenomenon in their samples, required obtaining germanium and the development of technologies to purify and grow germanium single crystals before turning again to silicon. This fascinating story and examples of research and technological challenges in silicon are reviewed by Kikuchi in *How Did a Physicist Fall in Love with Silicon in the Early Days of Japanese R and D?* Takao Abe will review research at SEH in silicon crystal growth technology in *A History and Future of Si Crystal Growth*. The control of carbon, nitrogen, oxygen, and metal impurities, crystal perfection, the role of residual point defects (vacancies and interstitials), and their interactions with the above impurities in forming chemical-structural complexes in both Czochralski and Float-Zone crystal growth will be discussed. New approaches to the growth of 300 mm and larger diameter crystals, and defect minimization as well as new dislocation-free seeding methods will be introduced.

Materials issues and IC fabrication. — The development of silicon material technologies during IC fabrication, supporting the transformation of the fledgling microelectronics industry into a global behemoth (with a 25-30% compound annual growth rate) will be reviewed. Concurrently, the number of transistors per chip has increased with a compound annual growth rate of approximately 40% such that the number of transistors is over 10 million on a state-of-the-art microprocessor (2). This enables a 25-30% per year cost reduction per function. The evolving path from germanium to silicon, especially regarding the importance of the surface properties, will be traced by Michael Riordan of Stanford University in *The Path to Silicon Was Paved with Germanium*. Ralph Bray's 1997 article

reviewing *The Invention of the Point Contact Transistor: A Case Study in Serendipity* (3) will be included to complement Riordan's article. Bray's article includes his experimental observations on germanium, as a member of the Purdue group during 1942-1945, which subsequently were interpreted as indicative of point contact injection. Bruce Deal, of Stanford University, retired from Fairchild, will discuss *Highlights of Silicon Thermal Oxidation Technology*. The role of silicon dioxide as a passivating layer for exposed p-n junctions, stabilization of the silicon interface, concomitant with a detailed understanding of the interface charges and the source of MOS instabilities due to the alkali ions (especially Na^+, along with K^+ and Li^+) and as a dielectric for overlying metallic conductors will be reviewed. The historical thread, from fundamental research on silicon surface passivation and the properties of silicon dioxide at Bell Laboratories, to what eventually became known as the planar process developed at Fairchild, is traced along with the utilization of silicon dioxide as an active participant in the MOS transistor. The linear-parabolic Deal-Grove oxidation model will be discussed along with consideration of the continuation or combination of silicon dioxide with other dielectric materials as the MOS gate dielectric in future ICs. Else Kooi, retired from Philips Research Laboratories, will review the development of the Local Oxidation of Silicon (LOCOS) in *The History of LOCOS*. The recognition that silicon nitride could be used to prevent oxidation of the underlying silicon during thermal processing led to the achievement of increased device densities in MOS as well as in bipolar ICs. The requirements of improved process control, concurrent with reduced device dimensions, will be discussed in relation to a variety of conundrums encountered during LOCOS processing such as "bird's beak," "white ribbon," "oxidation enhanced diffusion," and a variety of "stress effects." Substitutes for LOCOS to further increase device density have continually been investigated; in that regard, the role of shallow trench isolation techniques for the fabrication of recessed field oxides in complex ICs will be discussed.

The next set of papers will examine the role of residual grown-in point defects, the formation of process-induced defects and their mutual interaction, as well as their characterization in silicon. Alfred Seeger of Stuttgart University and the Max Planck Institute

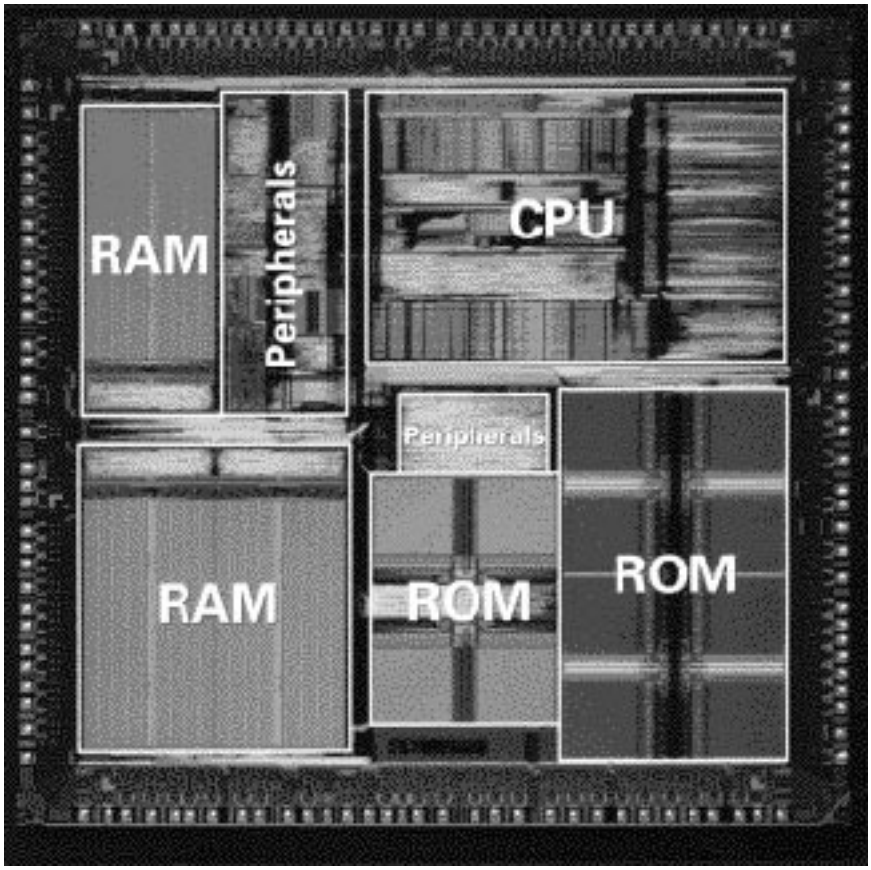

FIG. 3. A 1-Volt Digital Signal Processor—The device is created in a 0.35 micron triple metal CMOS process with 0.25 micron transistor gates. This DSP chip contains over 1.6 million transistors. (Photograph courtesy of Texas Instruments)

will describe *Self-Interstitials in Silicon*. The evolution of our understanding that self-interstitials are of fundamental importance (over and above the vacancy) for a host of solid-state phenomena in addition to diffusion will be reviewed. Ron Newman of the Imperial College of Science, Technology and Medicine in London will describe *Oxygen Aggregation and Interactions with Carbon and Hydrogen*. The importance of these microscopic reactions continues to be critical in controlling oxygen precipitation phenomena in silicon for gettering purposes, as well as a host of related phenomena. The ubiquitous role of hydrogen in a plethora of condensed matter reactions will also be highlighted. S.M. (Jimmy) Hu, retired from IBM, will review *Silicon Defects in Silicon Technology*. Processes such as crystal growth, thermal oxidation, nitridation and silicidation, impurity diffusion and ion implantation are critical IC fabrication steps which will be discussed as to their formation of non-equilibrium point defects which evolve into oxidation stacking faults (OSF) and dislocations. Structural inhomogeneities, such as film edges and trenches which can form localized stress fields large enough to cause dislocations, will also be reviewed. Oxygen precipitation phenomena, as to their effect on the silicon mechanical strength, will also be discussed. Gunter Schwuttke, Professor Emeritus of Arizona State University and retired from IBM, will describe *X-Ray Topography and Defect Control in Silicon IC Processing*. The control of dislocations introduced during crystal growth, wafer shaping and IC fabrication, and monitoring the synergistic effects of microscopic dislocation interactions and array configuration(s), will be described. Significant performance improvements will be highlighted for bipolar products by controlling dislocations introduced during diffusion (sub-collector buried layer, emitter edge dislocations), collector-emitter shorts (pipes), as well as thermally induced dislocations introduced into wafers during IC fabrication ramp-up/ramp-down procedures. Controlling plastic deformation continues to be applicable with the advent of the 300 mm diameter wafer era, due to the influence of gravitational deflection and stresses on thermal budgets for processing specific spatial configurations of wafers. George Rozgonyi of North Car-

olina State University, formerly with Bell Laboratories, will then describe the development of diagnostic techniques as a basis for *Silicon Wafer Defect Engineering*. These include methodologies for correlating structural defect patterns revealed by preferential etchants with electrical device parameters, including electron beam induced current delineated device defects precisely located by focused ion beam techniques in conjunction with TEM assessment, and the development of internal gettering to support reduced OSF, improved carrier lifetime and enhanced IC device parameters performance.

Materials issues and device/IC performance.—Jun-ichi Nishizawa, currently President of Miyagi University and Director of the Semiconductor Research Foundation and Professor Emeritus of Tohoku University, will describe *Key Advances in Si Device Physics and Technology*. The development of IC process technologies from a Japanese perspective and their integration into the emerging LSI and ULSI arena form a compelling narrative. Nishizawa's work on the Si thrysistor and the family of npin and pnip transistors will be described in detail. Yoshi Nishi of Texas Instruments will discuss his research on *Surface States and Device Performance* at Toshiba. The early phase of the MOS transistor involved the continuous struggle to control both fast and slow surface states to achieve stable device performance. Similar concerns for bipolar transistors indicated a significant dependence of the current gain with a controlled surface environment. The benefits of the increased control of surface states led to control of the MOS threshold voltage, subthreshold voltage characteristics and mobility in the triode region. Indeed, these characteristics continue to be of importance with the higher level of device integration fostered by reduced device geometries The increased understanding and control of surface states also prompted the invention of the metal nitride oxide semiconductor (MNOS) and floating gate non-volatile memory devices. The convergence of semiconductor technology, the replication of large numbers of identical transistor devices, and the rise of digital electronics will be shown by Jack Kilby, Texas Instruments, retired, to be significant drivers in the *Origin of the Integrated Circuit*. The invention of the IC (see FIG. 2) has expanded the microelectronics industry to an annual global revenue approaching one trillion dollars. Finally, Kiyoo Itoh of Hitachi describes *Pathways to DRAM Design and Technology for the 21st Century*. The impact of sub-threshold current and design parameter fluctuations of MOSFETs will be described in the context of CMOS scaling. Memory-cell scaling with reduced memory-cell leakage current, larger refresh time and high dielectric constant materials, as well as the potential of silicon-on-insulator (SOI) and alternative memory-cell configurations in the sub 100 nm technology generation will be discussed. Indeed, a number of these technologies for the fabrication of advanced DRAM configurations and, in a related fashion, microprocessors and digital signal processors (see FIG. 3) are impacting the evolution of the IC industry.

Silicon Symposium Program

The Silicon Symposium will also feature 31 additional invited papers distributed within eight sessions: Large Diameter Crystal/Wafer Issues; Wafer Preparation; Dielectrics, Interfaces and Epitaxy; Microscopic Physics Issues & Modeling; Gettering Phenomena; IC Process Integration; Alternative Material Systems; and Diagnostic Analysis. Sixty-two contributed papers delving further into the details appropriate to the sessions will also be presented. Both the invited and the contributed papers will present generally evolutionary outgrowths of the directions presented in the *Fifty Years and Counting* historical session. Newer topics will also be discussed, however, such as invited papers on 300 mm diameter wafers by Semiconductor Leading Edge Technology (SELETE) and the International 300 mm Initiative (I300I), 400 mm diameter wafers by the Super Silicon Initiative (SSI), developments in high permittivity ferroelectric materials with silicon, and evolving opportunities in SOI. The complete silicon symposium program is summarized in the program section of this issue. ■

References

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About the Author

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