TECH HIGHLIGHTS

Laser Crystallization of Amorphous-Si Thin Films

The fabrication of polycrystalline Si thin-film transistors is a key technology for active matrix liquid crystal displays (AMLCDs), large-area electronics, and vertically stackable components for 3D integration. Today, many of the commercially available AMLCDs use amorphous-Si (a-Si) transistors. However, the channel mobilities for a-Si are quite low, typically < 1 cm^2/V s, while polycrystalline Si offers significantly higher mobilities. One method for improving mobilities for polycrystalline Si is to use an annealing step, such as excimer laser annealing, to maximize the grain size in the crystallized a-Si. Viatella, Lee, and Singh at the University of Florida are studying the microstructural evolution of crystallized films annealed using a variety of masking techniques and laser energy densities. They found three types of microstructures. Samples processed with low energy densities resulted in a "standard" microstructure, having small, ~200 nm grains. Samples processed at higher energy densities demonstrated either enlarged grain growth (three times larger than the standard) or "anomalous" grain growth, where grains at the corners of the exposure area were approximately 1-2 μm in size. The authors also describe a semiquantitative, one-dimensional heat flow model of the crystallization process to explain these microstructures.

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Electrochemically Synthesized Nanostructures

Nanostructured materials are of interest for a number of applications, and much of the current effort in this area is aimed at development of synthetic preparation techniques. Researchers at CNRS in France have described an electrochemical method for preparing cobalt and iron nanowires and nanotubes. In their technique, a porous membrane is used as a template for structures that are electrochemically deposited using various pulse profiles. The versatility in this technique resides in the fact that the type of structure formed, *i.e.* nanotubes *vs.* nanowires, as well as the crystal orientation of the wires in the structure, are dictated by the pulse conditions used in the deposition. Furthermore, seemingly minor variations of the pulse conditions, specifically the overpotential in the early stages of crystal growth, result in significant differences in the structure. For example, merely by changing the deposition overpotential from -1.5 V to -1.3 V in the 300 to 500 ms step of the pulse profile, the structure of the iron nanowires was altered from single crystal body-centered cubic to a multiphase structure. Similarly, by controlling the pulse conditions, nanowires or nanotubes could be preferentially prepared. The authors provide an explanation for the observed differences in structures formed as a result of the different deposition conditions.

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Electrodeposition of Copper in Vias and Trenches

For new generations of ultra large scale integration in integrated circuits, copper filling of sub-micron vias and trenches will generally be accomplished using electrodeposition. Non-uniform potential fields and depletion of copper ion near the vias and trenches can cause non-uniform deposition resulting in voids in the copper interconnects and trapped plating solution in these voids. Takahashi and Gross at Bell Laboratories, Lucent Technologies in New Jersey developed a finite element model of the governing transport equations for electrodeposition into sub-micron features to determine the effects of copper ion transport and potential field on plating uniformity. The authors found that the most important effect leading to deposit non-uniformity was diffusion of copper ions through the plating solution. Convection in the sub-micron vias and trenches was found to be too weak to contribute to the mass transfer of the copper ions. Because of the importance of diffusion, they concluded that changes in fluid flow rate or solution conductivity would be unlikely to result in significant changes in deposit uniformity. However, changes in plating current density, plating waveform, or copper concentration would be more likely to result in changes to the via and trench properties.

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Ultrasmooth GaN Surfaces

Gallium nitride has emerged as one of the most promising materials for short-wavelength optoelectronics and high power microwave and radio frequency electronics (Ed. Note: See feature article in this issue.) The development of device processing techniques for GaN (as well as other III-nitride materials, *e.g.*, InAlGaN) has been crucial to the fabrication of a variety of discrete, high performance devices such as blue and ultraviolet light-emitting diodes, laser diodes, photodetectors, and transistors. Researchers at the University of Texas at Austin and the Air Force Research Laboratory in Ohio have reported a photoelectrochemical wet etch process that produces highly smooth GaN surfaces with minimal surface damage. The authors used aqueous solutions of potassium hydroxide and ultraviolet light to etch GaN layers grown on sapphire substrates. Smooth surfaces with root-mean-square (rms) roughnesses of ~4 nm were obtained within a narrow range of the etch process parameters. Outside of this narrow parameter space, whisker growth was observed on the GaN surface. These whiskers were easily removed by ultrasonic treatment in aqueous KOH, producing even smoother surfaces (rms roughnesses < 1 nm). Development of these kinds of wet chemical processes is essential to improved performance of devices that exploit the excellent optical and electronic properties of III-nitride materials.

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Macropore Formation in n-Type Silicon

Porous silicon (PS), typically formed by anodization of crystalline Si in hydrofluoric acid, has been extensively studied since it was first reported in 1956. PS has been used in chemical sensors, microelectromechanical structures, fabrication of silicon-on-insulator substrates, and compliant substrates for silicon and compound semiconductor epitaxy. In addition, some forms of PS exhibit strong photoluminescence, which has led to research aimed at eventual development of optoelectronic devices. It is well known that the density and microstructure of the porous layer can be tailored by appropriate choice of the anodization parameters. However, PS formation mechanisms are still being debated. Researchers at Christian-Albrechts University in Germany have described a detailed study of the mechanism of macropore formation in n-type silicon substrates. The authors report that a prolonged nucleation phase precedes the more rapid pore formation process. For low-doped n-Si, macropore formation proceeds in accordance with existing space-charge models. For highly-doped n-Si, pore growth appears to be controlled by a mechanism involving passivation of the pore walls.

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