Photons to the Rescue:
Microelectronics Becomes Microphotonics

by L. C. Kimerling

The evolution of the information age is being paced by the introduction of new materials and components more than by the design of systems, software, and networks. A rebuilding of the world's information infrastructure is taking place to give instantaneous availability of data, voice, and video. Electrons transmitted through metal wires have an information carrying capacity that is limited by the resistance and capacitance of the cable and the terminating electronic circuits. Photons transmitted through fiber are capacity-limited only by the dispersion of the medium. Each network node that requires transduction from photonics to electronics limits the performance and affordability of the network. A key frontier is the large scale integration and manufacturing of photonic components to enable the distribution of high bit rate optical streams to the individual information appliance.

The Interconnection Bottleneck

It is now one-half century since the invention of the transistor and the advent of solid-state electronics. Through unparalleled gains in functionality at relatively constant cost, integrated circuits have enabled telecommunications, computation, and manufacturing to move to the leading edge of societal change. This revolution has been conducted with the turn of a single knob—the shrinking of device dimensions. What is known today as "technology shrink" has increased computational speed due to shorter gate widths, and increased functionality through higher levels of integration and decreased costs by producing more transistors/chip and more chips/wafer. The driving forces for silicon electronics technology have been higher computational speed and functionality at lower cost.

The increase in integrated circuit performance has been exponential in time at rates of more than 100/decade. Such a pace represents the overwhelming impact of a "killer technology."[1] However, as critical dimensions have shrunk, the metal interconnection lines that provide the communication paths between devices have become smaller and more closely spaced to limit performance. This constraint is reflected in the increasing gap between the gate delay (switching speed) of a transistor and the propagation delay between transistors of an integrated circuit (see Fig. 1).[2] The introduction of copper lines and low dielectric constant insulating layers gives only a factor of four potential improvement at great risk to manufacturing yield and cost. This limit to chip performance is termed the "interconnection bottleneck." As Fig. 1 shows, a factor of four will delay the bottleneck for at most two generations to the 0.13 µm technology.

During the last two decades a new killer technology has emerged in the telecommunications field. This photonic technology uses optical fibers for interconnection, and has delivered an exponential increase with time of information carrying capacity to the industry (see Fig. 2).[3] Photonics has provided unparalleled bandwidth to the backbone of the discrete, point-to-point long distance (wide area network, WAN) telephone line technology. However, the circuit architecture (central switching office) that worked so well for voice communications now limits the universal access

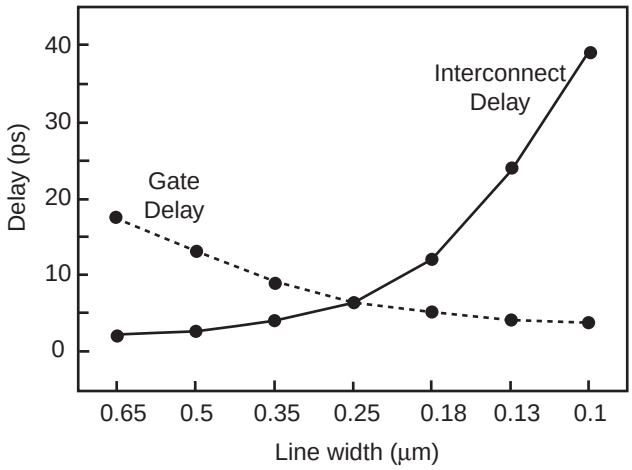


FIG. 1. Trends in transistor gate delay (switching time) and interconnect delay (propagation time for the Al/SiO_2 system) with integrated circuit fabrication technology. The cross over point represents the start of the "interconnection bottleneck."

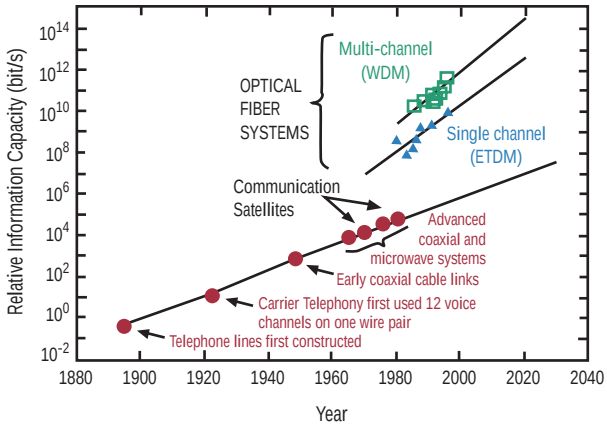


FIG. 2. Trend in information carrying capacity of a single line (wire or optical fiber) with time and technology. (WDM: wavelength division multiplexing; TDM: time division multiplexing).

that is required for Internet and data communications. A single optical fiber, with several hundred gigabits/second of capacity, is limited by electronic processing at each circuit node. To avoid this problem direct optical connections are required: optical cross-connects and optical add/drop multiplexers. To provide full functionality, these components must be integrated at densities compatible with current microelectronic integration. This microphotonics platform represents not only a solution to information access, but it can also solve the problems of bandwidth, pinout density, reliability, and complexity that threaten to end the advance of the silicon integrated circuit technology.

Microphotonics

The key enabler for microphotonics is confinement of the optical carrier to submicron device dimensions. Optical confinement is analogous to the particle-in-a-box problem in quantum mechanics. The high potential walls of the box are equivalent to a high index difference between the optical waveguide core and its cladding. The industry standard carrier wavelength is $\lambda = 1.55\ \mu m$. In an optical waveguide this dimension is λ/n_r, where n_r is the refractive index of the guide. Thus, high index waveguide media are necessary. This requirement is contrary to fiber optic technology, where low index SiO_2 ($n_r = 1.5$) is the medium. Transmission loss by light scattering is roughly proportional to $(\Delta n_r)^2$. For fiber optics technology $\Delta n_r \sim 0.01$ to minimize loss, whereas high confinement requires $\Delta n_r > 1$ to minimize size and enable large scale integration. As a rule of thumb, microphotonic device dimensions scale with Δn_r. Thus, for $\Delta n_r = 1$ a photonic device can shrink to an area of $(0.01)^2$ or 10^{-4} the size of a comparable fiber optic device. For simplicity this paper will concentrate on the use of silicon, $n_r = 3.5$, as the high index medium. Figure 3 shows a typical silicon waveguide cross-section for single mode transmission at $\lambda = 1.55\ \mu m$. Most of the commonly used semiconductors, GaAs, InP, and Ge have similar large values of n_r.

Microphotonic Systems and Components

There are no physical limits to the introduction of an all optical interconnection technology platform. In fact, the optical platform may be the only one that is scalable to an orderly evolution of future generations. It is unlikely that the microphotonic platform will consist of directly integrated discrete devices (sources, detectors, and waveguides) in a point-to-point architecture. Optical sources (semiconductor lasers), whose power, spectral purity, and temporal distortion performance have dominated WAN architecture design, may become the least critical component. Consider the optical bus architecture shown in Fig. 4. A photon bus supplies photons to the circuit form a central source in much the same way that a traditional power supply provides electrons. These photon streams can be switched, modulated and wavelength-converted to provide clock signals, to encode data and to route signals. In addition, they can be wavelength multiplexed to reduce pin count. Thus, waveguides, modulators, optical filters and switches and optoelectronic detectors rise in relative importance to distributed, discrete sources. For silicon microphotonics, a minimum materials set of Si, Ge, and SiO_2 can perform most of these functions.

Silicon Microphotonics

Silicon microphotonics utilizes silicon-based materials that are process compatible with standard integrated circuit fabrication methods. This approach has the support of the huge imbedded materials and processing knowledge base that supports the integrated circuit microelectronics industry. Microelectronics engineering is structured to meet the constraints posed by carrier transport and lifetime, and electric field design criteria. One is concerned with the control of scattering sites, recombination centers and localized sources of dielectric breakdown and leakage current. Microphotonics focuses concern on photon creation, propagation, and optoelectronic transduction. The figures of merit for photonics are optical power insertion loss, quantum efficiency of photonic/electronic transduction, and optical microcavity quality factor, Q (photon lifetime). Photon absorption and scattering are sources of loss. Localized dipole coupling determines the efficiency of photon generation and detection. Because optical modes and resonances are dimensionally determined, precise dimensional control at length scales of the photon wavelength in the medium is more critical for photonics than for electronics.

A good overall figure of merit for the performance of microphotonic integrated circuits, relative to all electronic or hybrid counterparts, is (speed)/(power x area). In addition, cost reduction and reliability are expected benefits integration. For example, an evaporated interconnect on a complex microelectronics chip has better reliability than a copper cable for telecommunications at about 10^{-12} of the cost! The following sections will review principles and prototypes of silicon microphotonics media, and active and passive components.

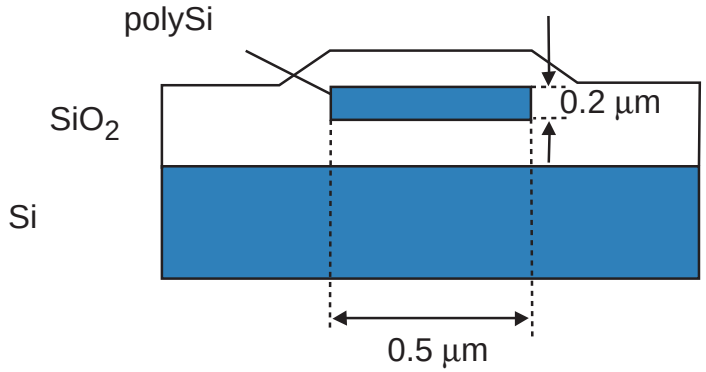


FIG. 3. Cross-sectional view of a polycrystalline silicon optical waveguide designed for a single mode propagation of $\lambda = 1.5\ \mu m$ light. The standoff from the silicon substrate is 0.7 µm.

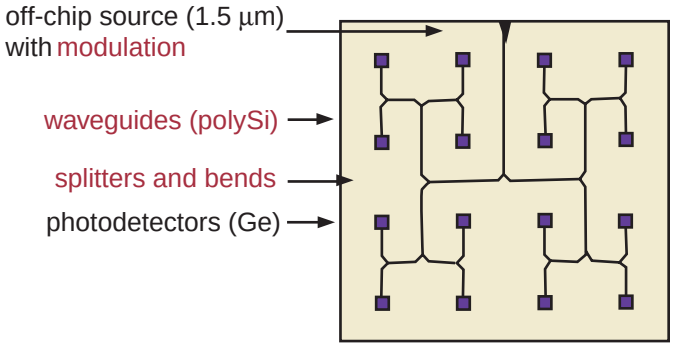


FIG. 4. Schematic diagram of an optical bus architecture for global clock distribution.

Silicon Microphotonic Waveguides

The main challenge of silicon microphotonics lies in reducing device sizes to dimensions comparable to integrated circuit electronics while utilizing CMOS compatible processes. Typical optical fiber and planar waveguide structures feature $\Delta n = 0.01$ by doping of the SiO_2 waveguide core with Ge or P. This relatively weak confinement limits not only device size, but also the ability to navigate photons around the sharp turns required for intrachip optical interconnection. Turn radii of less than a millimeter yield high radiative loss. Alternately, a Si core clad by SiO_2 waveguide structure exhibits a $\Delta n=2$, and the linear scaling factor of 200 allows turn radii of one micrometer. The Si/SiO_2 materials system with $n(Si) = 3.5$ and $n(SiO_2) = 1.5$ meets all the requirements for microphotonic waveguides. Silicon is transparent for $\lambda = 1.3\text{-}1.5$ µm photons, and the index match to semiconductor emitters and detectors is ideal for low insertion loss. However, high index contrast structures present a process problem, because performance is limited by scattering loss from surface roughness.

Silicon-on-insulator (SOI) platforms are required to prevent power loss to the silicon substrate. High performance strip waveguides (see Fig. 3) are dimensioned at 0.5 x 0.2 µm for single mode transmission in the $\lambda = 1.3\text{-}1.5$ µm range. A 7000 Å SiO_2 cladding isolation from the underlying silicon substrate is required. A single crystal silicon waveguide can be fabricated by wafer bonding approaches to give flexibility in layer thicknesses with a high quality, silicon transmission medium. Polycrystalline silicon offers the maximum flexibility in layer positioning as well as thickness. The materials engineering challenges are reduction of sidewall roughness to limit optical loss and process integration to maintain dimensional integrity and microelectronic compatibility.

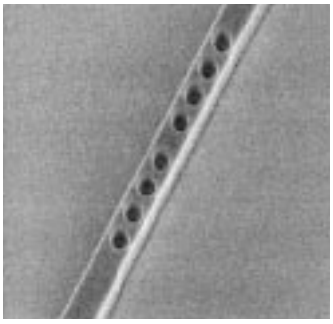
We have fabricated micron-sized, polycrystalline silicon bends and splitters based on submicron waveguide cross-section dimensions with low loss. With Y-splitters and bends, we fabricated the first 1x4 and 1x16 fanout optical power distribution using poly Si waveguides. Our 1x16 fanout optical system occupies an area as small as 0.0001 cm^2, which is the smallest such fanout system ever built.[4] A 1x8 splitter based on a multimode interference (MMI) design has yielded our smallest and most efficient 1x16 splitters to date. These nanowaveguide structures also allow construction of microring resonator devices that act as wavelength division multiplex (WDM) filters and routers.[5] Data from a micro-ring cascade for WDM demultiplexing have shown excellent channel separation, made possible by wide free spectral range of micrometer-dimensioned ring resonators. The miniaturization and integration of these optical routing devices and systems constitutes the basic foundation for the microphotonics platform.

Photonic Crystals

Photonic crystals are composite materials that consist of a periodic lattice of high and low refractive index materials. The refractive index variation acts in a similar fashion to atomic lattice potentials in semiconductor materials. In photonic crystals a band of energies exist for which no photons can propagate (similar to the electronic bandgap of semiconductors and insulators). The higher is the index contrast, the larger is the bandgap. The bandgap represents a frequency range of perfect reflection. A defect in the photonic crystal, such as a vacancy or missing high index component on a lattice site, constitutes a deep level that traps photons. The binding energy of the trap is equivalent to the Q factor of the photonic microcavity. These materials and photonic defects have been engineered to produce the world's smallest microphotonic components.

Figure 5 shows the structure and transmission spectrum of a one dimensional PBG structure with a photonic defect.[6] The structure is composed of a 0.5 µm wide silicon waveguide with a series of periodically spaced air holes to create the photonic band gap. A missing air hole in the center is the defect. The bandgap was designed to span the amplification spectrum of the industry standard SiO_2:Er fiberoptic amplifier. The defect acts as a photon tunneling state with the width of the pass band being inversely proportional to the Q factor of the defect microcavity. This device functions as a channel drop filter for WDM applications. The device performance closely follows the PBG design, and the measured Q of 250 is capable of fitting 128 different wavelength channels within the amplifier spectrum. The optical mode volume of the device, 0.0552 μm^3, is the smallest ever created.

Photonic crystals represent a new silicon process challenge. The periodicity of the microstructure is the major performance constraint. Air holes and Si/SiO_2 multilayers in one dimension, post arrays in two dimensions, and displaced checkerboards in three dimensions have been addressed by a variety of approaches. The multilayer structure research closely parallels the development of 3-D SOI integration of electronic circuits. Wafer bonding,[7] chemical vapor deposition (CVD), and sputter deposition have been successful, because the high index contrast of the materials system requires only four layer pairs (GaAs/AlGaAs requires many tens of layer pairs) for a sufficiently high cavity Q. The critical dimension for light of $\lambda = 1$ µm is of the order of 0.1 µm for silicon with a tolerance of ± 0.01 µm. This dimensional regime is highly desirable for microphotonics, and the capability to achieve these dimensions with routine silicon fabrication-line processes is likely within the next five years.



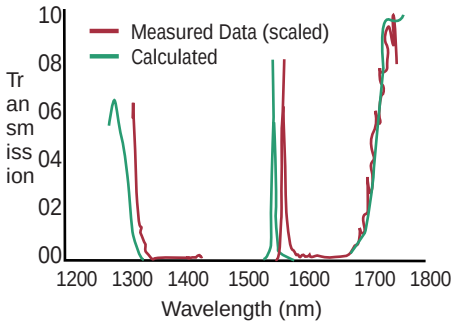


FIG. 5. Structure and performance of a 1D photonic crystal resonator. The structure consists of air holes in a 0.5 µm wide silicon waveguide.

Detectors

Transduction of photons to electrons is required for the integration of microphotonics with microelectronics. Because photons of energy greater than the silicon band gap can be absorbed throughout the integrated circuit, and inject spurious signals, "sub-gap" energies are preferred. Materials with

bandgaps less than the photon energy must be used for detection. The primary candidate for monolithic integration with silicon is the SiGe alloy. Band structure calculations have defined the design window for these alloys.[8] For high speed and high levels of integration small detector sizes and short absorption lengths are desired. Pure Ge can provide absorption coefficients for λ = 1.3-1.5 µm photons that are comparable to direct gap compound semiconductors. The defect engineering challenge is accommodation of the 4% lattice misfit between the Si substrate and the Ge layer. Planar misfit dislocations are acceptable in a passive region of a photodetector, but threading dislocations that extend through the active region are sources of leakage current and recombination that reduce responsivity and introduce noise to the detector performance. We have fabricated and tested heterojunction Ge photodetectors based on Ge epitaxially grown on Si (001) using a two-step ultra-high vacuum-CVD process followed by cyclic thermal annealing. For selective area growth of 100% Ge on Si, the multi-step deposition and anneal sequence produces threading dislocation-free Ge material.[9] As shown in Fig. 6, the detectors exhibit typical responsivity of 550 mA/W at 1.32 µm and 250 mA/W at 1.55 µm. Response times shorter than 850 ps were measured at 1.32 µm.[10] Novel process schemes such as these are critical to the introduction of a monolithic microphotonics technology platform.

New Materials and Processing Paths for Microphotonics

A range of new processes are being considered to meet the stringent dimensional constraints of microphotonics. Photonic crystals offer the ultimate in control of photonic functions, but the need for an artificial, periodic composite microstructure makes pattern transfer approaches difficult. Self-assembly techniques are the most promising alternative path to generate such structures. Recently, colloid aggregation and phase separation in block copolymers have been adapted to the needs of microphotonics.

Colloidal aggregation can lead to a close packed lattice of spheres that can be the building block for a three dimensional photonic crystal. In the limiting case of a two dimensional structure made with this approach, electrostatic adhesion, promoted by charged polyelectrolytes, is used to create a selective, stable array of dielectric spheres. Both SiO_2 and polystyrene spheres with micron and submicron dimensions have been employed.[11]

Block copolymers phase segregate into periodic microstructures with length scales determined by the polymer segment lengths. By adding homopolymer, the optical response can be controlled by swelling of the periodic microstructure. Systematic changes have been observed in the reflectivity of a polyisoprene/polystyrene block copolymer as styrene and isoprene homopolymers are added.[12] For block copolymers with one block possessing a silicon backbone and the other a carbon backbone, oxidation leads to a periodic SiO_2 lattice as the carbon is volatilized to CO_2.[13] The above self-assembly processes offer promising paths for the growth of photonic crystals at low cost.

Summary

The microelectronics age has been characterized by an exponential growth in the performance of electronic systems at relatively constant cost. The benefits have been primarily in the form of faster, more available computation hardware. The information age has been ushered into existence by this high quality database. The future of the information age lies in the networking of databases for universal availability, that in turn will require a mating of microelectronics and fiberoptic technology with microphotonic interconnection. ■

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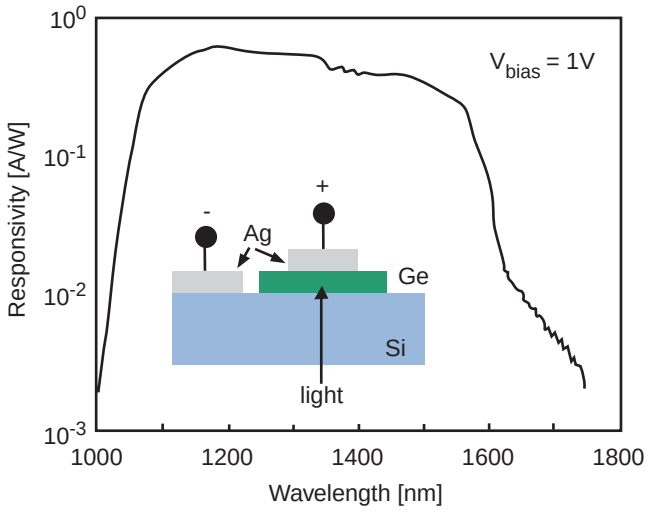

FIG. 6. Performance of a p-i-n germanium on silicon photodetector. The device was fabricated by direct growth with low dislocation density.