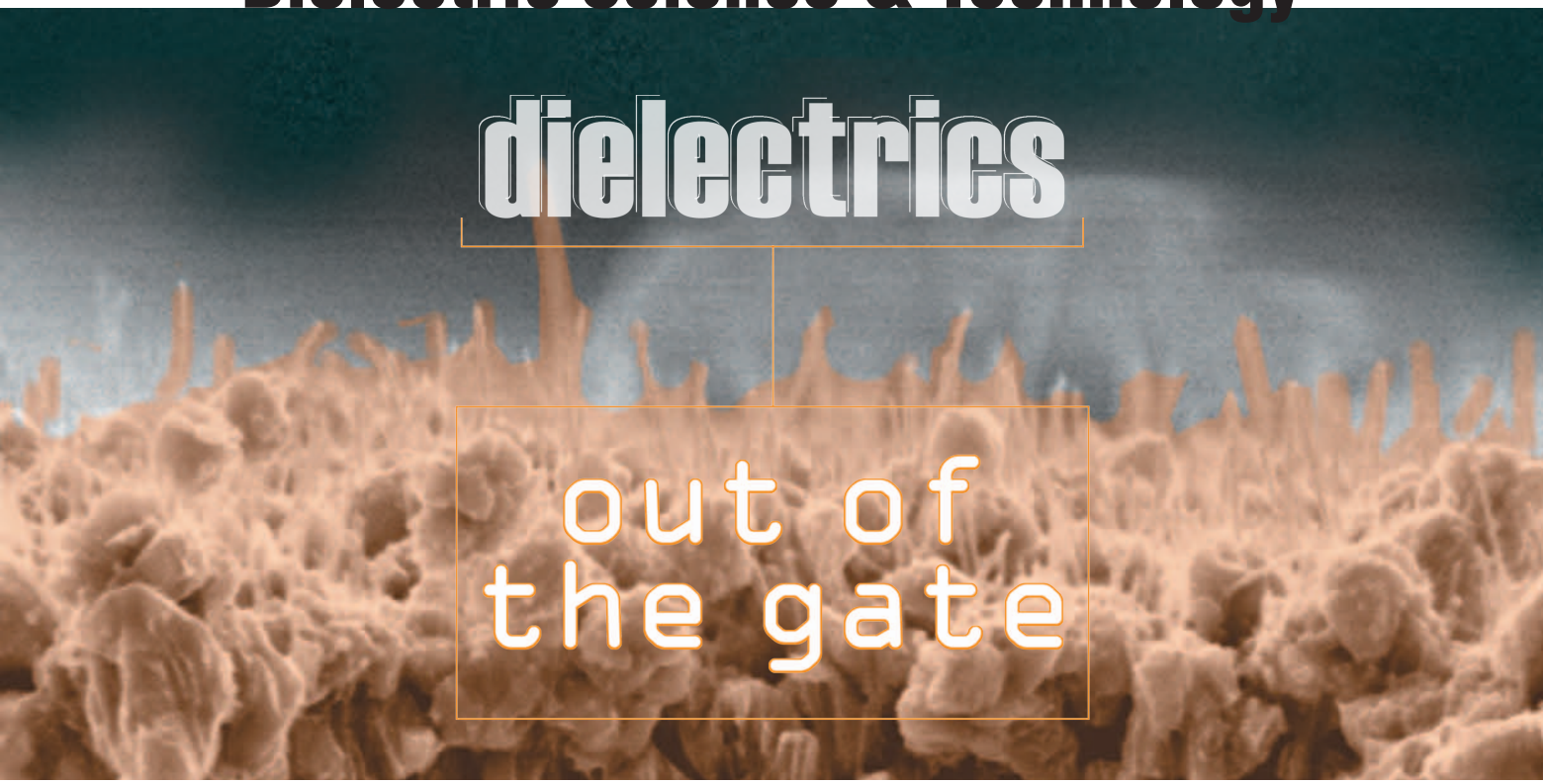
Dielectric Science & Technology



by M. Jamal Deen

The recent explosion in wireless and information technology has been one of the most dramatic applications of semiconductor technology in the past decade. This explosive revolution is apparent in the ever increasing use of wireless products such as cell-phones, personal digital assistants (PDA), digital cameras and electronic entertainment systems. Key ingredients of this technological revolution have been the rapid advances in the quality and processing of materials, and in device, circuit, and system design and integration. In the area of materials, the science and technology of dielectrics occupies a prominent place in providing the dominant technology, complementary metal-oxide-semiconductor (CMOS), with its important characteristics of negligible standby power dissipation, good input-output isolation and surface potential control for switching operations.

In mainstream silicon semiconductor technology, silicon dioxide is particularly important. One key reason for this is the ease with which high-quality, thin films of silicon dioxide can be grown on silicon surfaces to create MOS transistors. In addition, silicon dioxide is used for device and interlevel metal isolation. However, with the continued miniaturization of silicon MOS transistors, not only is the channel length L_{eff} reduced to very small values, but the equivalent oxide thickness (EOT) of gate dielectric is also reduced to below 1 nm to maintain adequate control of the inversion layer for good device operation. Figure 1 shows this evolution out to 2009 for both L_{eff} and EOT.

However, with this decreasing oxide thickness, gate tunneling currents become important. This is nicely shown in Fig. 2 where the gate tunneling current density is plotted for the same time out to 2009. It shows that after 2006, just one year away, a proverbial red-brick wall will be reached in which the gate current density will exceed the limit set by the power dissipation considerations. To circumvent this problem, researchers are actively investigating novel dielectrics with higher dielectric constants so that thicker oxides can be used to reduce the gate current densities, while

(continued on page 58)

Upcoming DS&T Sponsored/Co-sponsored Symposia

Los Angeles, California • October 16-21, 2005—Dielectrics and the Dielectric/Electrolyte Interface in Biological and Biomedical Applications; Thermal and Plasma CVD of Nanostructures; High Dielectric Constant Gate Stacks III; Atomic Layer Deposition Applications: Challenges and Opportunities; Copper Interconnections, Low-k Interlevel Dielectrics, and New Contact and Barrier; Physics and Chemistry of SiO_2 and Si-SiO_2 Interface V; Cleaning Technology in Semiconductor Device Manufacturing IX; Thermal and Plasma CVD of Nanostructures.

Denver, Colorado • May 7-12, 2006—Thermal and Plasma CVD of Nanostructures; Environmentally Conscious Microelectronics Manufacturing; Plasma Processing XVI; Dielectrics for Nanosystems: Materials Science, Processing, Reliability, and Manufacturing II.

Cancun, Mexico • October 29-November 2, 2006—Chemical Mechanical Polishing VII; Science and Technology of Dielectrics for Active and Passive Devices; Dielectrics and the Dielectric/Electrolyte Interface in Biological and Biomedical Applications; High Dielectric Constant Materials IV; Molecular Structure of the Solid-Liquid Interface and Its Relationship to Electrodeposition V; Advanced Gate Stack, Source/Drain, and Channel Engineering for Si-Based CMOS: New Materials, Processes, and Equipment II.

(continued from page 29)

still maintaining good control of the inversion layer. Concurrently, these novel dielectrics should satisfy the *International Roadmap for Semiconductors* (ITRS) device reliability requirements and be easily integrated into the technological process to create low operating and low standby power MOS transistors. Other important requirements such as good surface and interface integrity with the different materials over the entire device fabrication process are of paramount importance, in addition to the cost of the process changes. In addition, low dielectric constant materials are required to reduce the delay time due to interconnection parasitic capacitances in current and future highly integrated electronic systems.

The above discussion is not intended to suggest that dielectric science and technology (DS&T) is only important for electronic components. Far from it – in fact, dielectrics play important roles in a variety of applications ranging from sensors, isolation for conductors in the power utility industry, to ceramic cookwares. Further, in the rapidly emerging field of biological systems, the dielectric constant is important since electrostatic effects are used to link structure and function of biological molecules. It has been proposed that electrostatic effects play a major role in important biological activities such as enzyme catalysis, electron transfer, proton transport, ion channels, and signal transduction. It is expected that the DS&T Division will play an increasing role, in collaboration with other Divisions in ECS, in promoting the varied and important role of the science and technology of dielectrics in existing fields of sensors, nanotechnology, electronics, photonics, chemical and mechanical systems, but also in emerging fields of biology and biochemistry.

In this issue are articles discussing three important aspects of dielectric science and technology. The first deals with high dielectric constant dielectrics for gate insulators. It discusses the current status and important electrical and reliability issues of these dielectrics. The second article is an update on low dielectric constant insulators that are particularly important for isolation of interconnects. The third article, also forward-looking, discusses future prospects and applications of carbon nanotubes and inorganic nanowires.

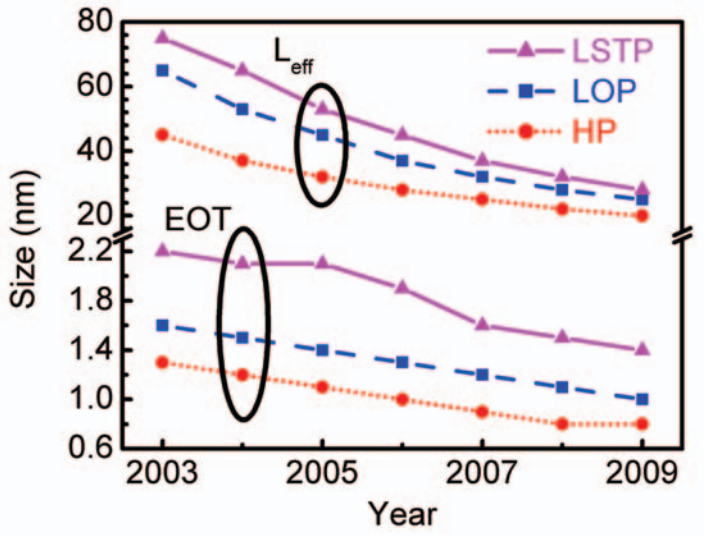


FIG 1. Decrease of the effective channel length (L_{eff}) and equivalent oxide thickness (EOT) with year according to ITRS 2004 for high performance (HP), low operating power (LOP), and low standby power (LSTP) technologies.

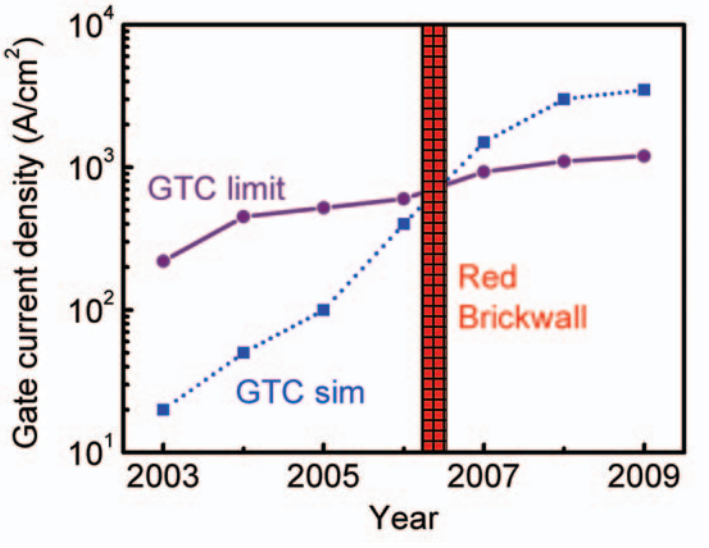


FIG 2. Simulated gate current density and practical gate current density limit as a function of time for silicon oxynitride gate dielectric from the ITRS 2004. Note that after 2006, the practical gate current limit is exceeded, thus requiring novel gate dielectrics with higher dielectric constants.

I sincerely hope that you too will enjoy reading these articles on key aspects of dielectric science and technology. ■

About the Author

M. Jamal Deen is professor and Senior Canada Research Chair in Information Technology at McMaster University, Hamilton, Ontario, Canada. He is also Chair, Dielectric Science and Technology Division, The Electrochemical Society. He can be reached at jamal@mcmaster.ca.