Faraday in the Fab:

A Look at Copper Plating Equipment for On-Chip Wiring

by Christopher L. Beaudry and John O. Dukovic

It has been interesting to watch the growth and development of copper interconnects on silicon chips in the seven years that have passed since IBM announced that it would use electrodeposited copper for the wiring structure of its 0.25-micrometer CMOS7 microprocessor.[1] *Interface* readers may recall Panos Andricacos' 1999 article, "Copper On-Chip Interconnects, a Breakthrough in Electrodeposition to Make Better Chips."[2] True to the prophecy, copper interconnect technology, enabled by the Damascene copper plating process, has steadily spread through the microelectronics industry and is now used throughout the world by manufacturers of advanced microprocessor and application-specific chips. The transformation has involved a tremendous amount of technical innovation, engineering effort, and capital investment.

This article treats only one small portion of the copper-interconnect universe, but it is a central one: the equipment used for electroplating. Admittedly, we take a somewhat plating-centric view, though we do not want to diminish the importance or complexity of the other steps in the interconnect-fabrication sequence. Ironically, one could argue from an economic perspective that, of all the major steps in the Damascene processing sequence: dielectric deposition, lithography, etching, barrier/seed deposition, plating, and chemical mechanical polishing, plating is among the least important because its cost is relatively low by comparison. To this we answer, first, that low cost is generally a good thing, and we point out the inescapable fact that plating is the step that actually forms the copper lines and vias, *i.e.*, it is the plating tool that puts the copper on the wafer (except for the seed layer). Plating equipment, however central or important, is an interesting story in itself. The growth of the wafer-plating tool market is shown in Fig. 1. Annual sales are currently on the order of $200M with substantial growth projected over the next few years.[3] There are over 200 tools currently in use in semiconductor fabs around the world. One reason for this is that, to make a typical high-end microprocessor, the wafer passes through the plating tool 8 to 10 times, once for each level of the multilevel wiring structure, and the number of levels is increasing.[4]

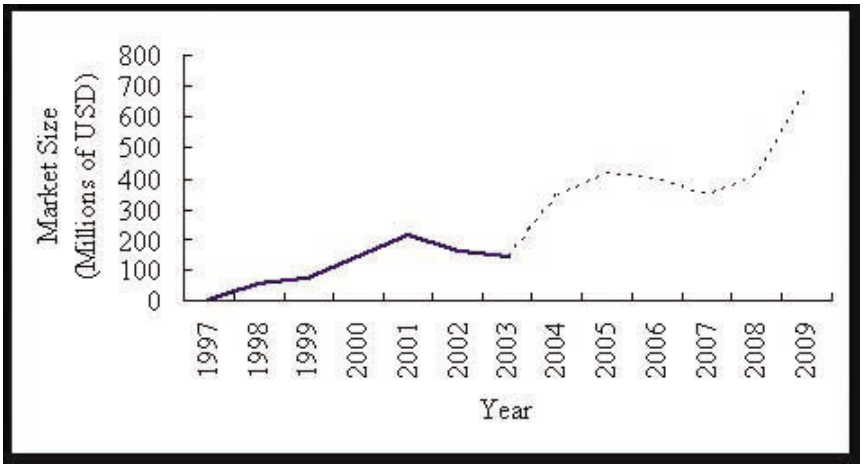

Fig. 1. Cu electrodeposition equipment market and forecast (Source: Gartner Dataquest July 2004).

Fig. 2. Applied Materials SlimCell™ System.

FIG. 3. A look inside the Applied Materials SlimCell™ System.

What's Out There?

Let us take a look at today's wafer-plating tools and consider some factors that have affected their design and some ways in which they are continuing to evolve to address new challenges in the industry. Sources of information on plating tools include the semiconductor trade journals,[5-10] the patent literature, and product information directly from tool suppliers.[11] Our purpose in this article is to present a smattering of information and perspective that we hope will be informative and interesting to a wide ECS readership. The content and reference citations are far from comprehensive. Also, although we have tried to be balanced and objective, our affiliation with one particular supplier of wafer-plating equipment disqualifies us from giving descriptions of tools other than our own and makes it nearly impossible for us to give an impartial view.

The external appearance of wafer-plating tools, such as that in Fig. 2, reflects their need to be accommodated in a modern semiconductor fab, in which there is great emphasis on particulate contamination, economy of space, efficient facility connections, and compatibility with automated transport of wafer pods from tool to tool. Generally, the front of the tool is the factory interface, where the wafer pods attach to the tool so that a robot inside the tool can remove one wafer at a time for processing inside the tool. Although plating is a wet process, the wafers are completely dry when they exit or enter the wafer pod. The fab is a clean room, but the air inside the tool mini-environment is even cleaner.

Inside the tool (Fig. 3) is an arrangement of chambers, each typically processing one wafer at a time. Some chambers are electroplating cells and others are locations where the wafers undergo prewetting, edge-bead removal, rinsing/drying, and annealing. The wafers are moved from chamber to chamber by a robot, which is typically not the same robot used in the factory interface. Accordingly, there is substantial mechanical complexity, and there is significant industry pressure for the tools to be highly reliable despite their complexity.

The main function of the tool is to provide the environment for the Damascene plating process to be carried out on the wafer. The process itself is paramount. The superconformal filling of via holes and trenches and production of void-free vias and lines is mainly the work of the organic additives in the bath. The superfilling effect (its discovery, elucidation, practical application, continuous improvement to meet escalating requirements) is an involved and fascinating story. At the risk of gross oversimplification, the mechanism envisioned by Andricacos and co-workers[2,12] has been largely supplanted by the curvature-enhanced accelerator coverage (CEAC) model,[13-16] although other views continue to be put forth and discussed.[17,18] Tom Moffat's paper in this issue of *Interface* addresses the present state of knowledge of superfilling.

Whatever the complexities of the superfill mechanism, from the standpoint of the plating cell and its requirements, the main practical objective is to permit the reaction to occur successfully at all points on the wafer surface and for every wafer processed. We know that the cavity-filling performance depends sensitively on the local electrochemical conditions, including overpotential and the concentrations of numerous species in the solution: the additives (typically the accelerator, suppressor, and leveler), reaction products of these additives, chloride ion, sulfuric acid, and cupric sulfate concentration. Accordingly, we know from electrochemical engineering principles (and common sense) that three conditions must be met by the plating cell:

1. The solution composition must be constant over time.
2. The overpotential at the wafer surface must be uniform at all points on the wafer surface and consistent from wafer to wafer.
3. Mass-transfer conditions must be uniform so that the local concentrations of species in solution adjacent to the electrode surface (*i.e.*, inside the concentration boundary layer) do not vary across the wafer surface.

These ideals, though not necessarily expressed this way, have been central to the design efforts that have shaped the plating cells that are in use today. For example, partly from consideration of mass-transfer uniformity, in today's plating tools the wafer is typically held face down in the electrolyte and is rotated during electrodeposition. Rotation also gives the practical advantage of canceling out sources of azimuthal nonuniformity in the current distribution. The arrangement is similar to the familiar rotating disk electrode (RDE), whose well-characterized mass-transfer rate is uniform under ideal conditions. Wafer-plating cells differ from the laboratory RDE in significant ways: length scale, contact rings that protrude below the plane of the wafer, bounding walls relatively close to the wafer, and forced flow (generally upward). The consequences of nonuniform mass transfer across the wafer include center-to-edge differences in (1) the cavity filling behavior (although this may be due to nonuniform current density as well); (2) the degree of overplating in zones with densely packed narrow trenches; and (3) the concentra-

tion of C, S, N, O, and Cl impurities in the copper. Accordingly, cells are engineered with avoidance of these center-to-edge differences.

Aside from the classical electrochemical-engineering issues of uniformity and composition control, there are many other requirements of great practical importance. For example, making electrical contact to the wafer is a highly nontrivial matter that involves considerations of contact resistance, repeatability, defects, prevention of damage to soft low-k dielectric films, minimizing the edge exclusion (the unusable area of the wafer), lifetime and cost of consumable parts, integrity of seals, and management of residues. This is one area where there are significant differences among tool suppliers. Another surprisingly nontrivial matter is the method of immersing the wafer into the plating solution. There are several kinds of killer defects that originate during wafer immersion. One such defect, sometimes called the swirl defect,[19] appears on the wafer as a cluster of voids in an arc pattern. Its occurrence is highly tool and process dependent. Some chip manufacturers mitigate the problem by using an additional rinse step prior to plating (a capability generally offered as an option by tool suppliers). Prewetting may not be necessary if the wafer is introduced into the solution with a motion sequence that does not trap air or result in uneven wetting of the wafer surface. A further complication is that it is typically necessary for the wafer to be held at a cathodic potential as it is being immersed so that corrosion of the copper seed layer is prevented. This is typically done by applying a fixed voltage to the cell during the brief period of immersion, before switching to the controlled-current mode used for the plating. It is a widespread practice to plate with low current density in the early stages of deposition (when most of the critical cavity filling is taking place) and to step incrementally to higher current density as the deposition proceeds.

Some Recent Developments

Let us consider several recent developments in plating equipment design that arose from special challenges of high-yield semiconductor manufacturing. We begin with specific measures taken to reduce defects and improve process control. Features that require defect-free filling are submicrometer in scale, becoming smaller with each design node[4] (approximately every two to three years), and that there are literally billions of these fine features on a 300 mm wafer. Thus, a very small particle can easily compromise the integrity of the interconnect wiring, potentially reducing device yield. One example of the many different kinds of defects that can occur at the plating step is the copper ball defect, pictured in Fig. 4. This particular defect is associated with copper fines that originate at the anode.

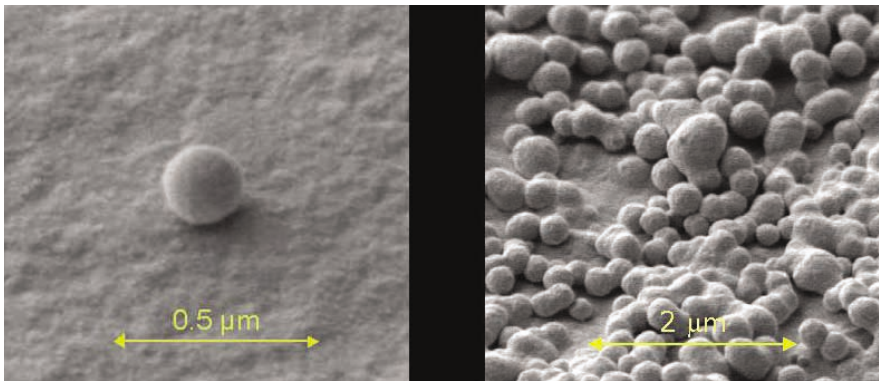

Fig. 4. Sample SEM images of typical Cu ball defects.

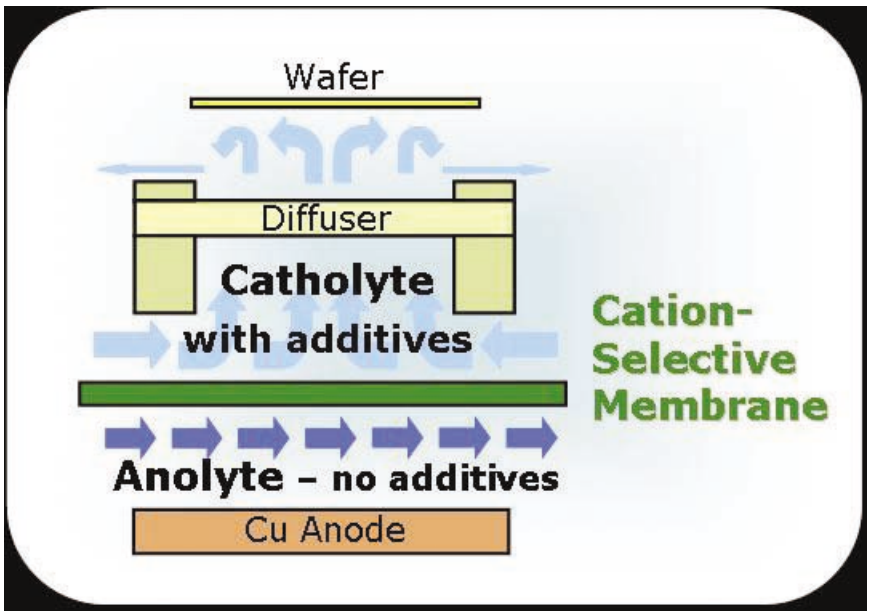

Fig. 5. Illustration of a plating cell using a cation-selective membrane to separate the anode and cathode (the wafer).

To date, all Cu electroplating tools in production use a cell design with a Cu anode. Anodes have historically been a problematic source of copper sludge and particles, which may release into the electrolyte and deposit on any wetted surface, including the wafer. The bath is typically recirculated through a filter, but this offers limited effectiveness. Various other means have been developed to reduce anode-related contamination, mainly involving porous separators, intended to physically retain the contamination on the anode side of the separator. Initially, these were made of woven cloth anode bag material, which later evolved into fine-pore separator materials. Recently, a cell with a cation-selective membrane separator was introduced to divide the electrolyte into two completely separate solutions, a catholyte in contact with the wafer and an anolyte in contact with the anode (Fig. 5).[20] While Cu ions can readily pass through, there is no fluid flow across the membrane. Accordingly, there is no way for particles originating at the anode (including those that cause the copper ball defect described above) to create defects at the wafer.

Another problem with anodes is that the organic additives, which are crucial to the electrodeposition process, undergo reactions at the anode surface. This is a copper surface to which the additives (by design) are prone to adsorb, and they can be consumed, especially during plat-

ing when it is at an oxidizing potential, but also at open circuit. There are three parts to this problem. First, it causes the additives, especially the accelerator, to be consumed, which increases the need for additive dosing. Second, since the rate of additive consumption depends on the anode's surface condition, which changes over time in response to utilization and idle periods, the consumption tends to be unsteady and unpredictable. Third and perhaps most significant, the reaction products, some of which are electrochemically active, accumulate in the bath and affect the electrodeposition process on the wafer. The conventional approaches to decreasing additive consumption at copper anodes are (1) to use phosphorized copper, which forms a black viscous sludge-like film and (2) to rely on the separator material to decrease the convective transport of the additives to the anode and of additive breakdown products from the anode to the wafer. The implementation of the cation membrane, described above, has resulted in a complete solution to the problem of additive reactions at the anode, because the additives are present only in the catholyte and are unable to cross the membrane and reach the anode. Moffat *et al.*[21] quantitatively demonstrated that separation of the electrolyte with a cation-selective membrane offers significant advantages in process stability by eliminating anode-related accelerator breakdown. By reducing the overall consumption rate of the accelerator, which has been demonstrated to be the additive most susceptible to breakdown,[22] it is possible to extend the useful life of the electrolyte.

Equipment suppliers have developed bath-control methods and hardware with the intention of extending the useful lifetime of the bath. From the basic requirements for superconformal filling, we must maintain all the organic additive concentration levels within the process window. Furthermore, it is also important to avoid any detrimental process impact of the accumulation of the numerous organic additive breakdown products, some of which are electrochemically active, which are generated during the plating process. For both reasons, the plating solution is periodically refreshed in an effort to restore the bath to the upper end of the organic concentration window and to minimize breakdown products. With this in mind it is interesting to explore the impact of hardware design on the methodology and capability of bath concentration control.

First-generation equipment designs followed the conventional plating-industry practice of using a relatively large bath, with 150-250 L of electrolyte recirculating to the plating cells. In such systems, the bath composition is typically maintained by replenishing the individual additives and using the "bleed-and-feed" method, in which a fraction of the bath (typically 10-30% per day) is regularly drained and replaced with fresh plating solution. This practice is used to limit the accumulation of additive reaction products and intermediates, which can be numerous[22] and which are linked to degradation in process performance, particularly gapfill. With continued downward scaling of via and trench dimensions, it is likely that breakdown products will pose an increased challenge to process stability. Although it is theoretically possible by proper application of the bleed-and-feed approach to obtain a steady state in which there is no variation in the concentration of any species, including breakdown products,[23] it is difficult to do this in practice. For example, one cannot count on having a steady plating workload day after day, so that charge-based and time-based reactions can occur at exactly proportional rates. Also, even under ideal conditions, the steady state is not reached until several residence times have passed. (At 10% bleed and feed per day, the residence time is 10 days.) Finally, for various practical reasons, bleed-and-feed baths are often dumped and replaced after a few months. An alternative approach, recently introduced,[9,20] is to use a very low bath volume (less than 15 L), to plate a finite number of wafers from this bath without bleed and feed, and then to replace the bath with a new solution. By this simple method, it is straightforward to prevent significant accumulation of breakdown products, and the need to monitor and dose the additives is virtually eliminated.

Interestingly, many of today's plating tools for Damascene copper contain a chamber for thermally annealing the wafer after plating. The overall importance of annealing the plated film to control grain size, stress, defects, and resistance to stress migration and electromigration is widely recognized.[24,25] However, because the effects of the annealing process are complex, with a dependence on many factors, such as electrolyte composition, plating condition, film thickness, dielectric material, wiring structure and process flow, there is a wide variation in the way annealing is used in practice. An anneal step longer than a few minutes is not straightforward for implementation on industry standard plating tools, which generally process a single wafer at a time with emphasis on high throughput. If a long anneal is needed, it is more practical for this to be done in batch fashion. However, if plating and annealing are done in separate tools, the queue time between plating and annealing will vary, and this may cause unwanted variation in film properties because grain structure and resistivity change significantly at room temperature over a period of hours to days.[2,26,27] Accordingly, one rationale for using on-board annealing is to stabilize the grain structure before the wafer leaves the plating tool. The present situation in the industry is that there is no consensus on whether to perform annealing on the plating tool, and the capability is offered by tool suppliers as an option.

Changes Ahead

Just as a person whose mental image of plating is a row of open tanks may be surprised to see how much has gone into the equipment used today for chip wiring, it is even more interesting to consider where things may be heading next. Because form inevitably follows function, we look to the semiconductor industry roadmap[4] to see what new requirements are expected. One certainty is that the dimensions of the cavities that must be filled by electroplating will decrease steadily for some time to come. There are many likely consequences to this downward scaling. The superfilling effect must work reliably in the narrower via holes and trenches. As superfill is the result of bath chemistry, with the tool playing an important role, we can expect the emergence of improved additives and an increased need for improved control of bath chemical composition (including plating by-products).

Another current concern is the extendibility of physical vapor deposition (PVD) to produce the copper seed layers in tomorrow's smaller cavities. Those seed layers must be thinner, and, unless great improvements in PVD-Cu step coverage are made, it may not be possible to achieve a robust continuous film of copper on the lower sidewall of the via to permit consistent nucleation of electrodeposition. Alternatives to PVD Cu nucleation layers are currently being explored. Notable among these is ruthenium, which is a good substrate for copper plating[28,29] and can be deposited by a highly conformal atomic-layer deposi-

tion (ALD) process. Figure 6 shows a micrograph from some recent work on superfilling in electrodeposition of Cu on Ru liners.[29] One challenge that non-Cu seeds pose to plating equipment is the terminal effect, the tendency for the current density to be nonuniform as a result of the Ohmic potential drop associated with conducting current from the wafer edge to the entire wafer surface through a thin, highly resistive layer of Ru. The sheet resistance of proposed non-Cu nucleation layers (*e.g.*, a 20 Å film of Ru) can be two to three orders of magnitude higher than that of today's seed layers (*e.g.*, a 1000 Å film of Cu). Straightforward extension of methods currently used to manipulate current distribution generally will not be adequate to combat the terminal effect on Ru. Future plating tools must overcome this difficulty.

There are several ways that electroless plating can come into use in chip metallization. There would be a radical change in the copper plating tool business if the copper fill step itself were done by electroless plating. While this possibility has long been discussed,[2,30] it does not appear likely to happen soon. The first likely mainstream use of electroless deposition will be for deposition of a barrier or capping layer on top of the copper lines after chemical mechanical polishing.[31,32] This step does not lend itself to direct integration on the same tool used for forming the copper lines, because the CMP process, performed on a separate tool, must come between the copper plating step and the capping step. It is possible that electroless plating could be used to deposit materials in the liner (for example, the barrier layer or an electroplatable layer), in which case it may be practical to perform one or more electroless steps on the same tool used for the electrolytic cavity filling step. It should be mentioned that concepts have been proposed for performing planarization in the plating tool, during or after electrodeposition itself.[33] There is always an attraction to getting more done in one tool, but there are many countervailing considerations including process flexibility, throughput matching, integration strategies of individual chipmakers, and total cost of ownership for the process sequence.

It is hard to predict what is coming next in plating equipment for microelectronics. Changes can occur quickly in the chipmaking industry. The cost of making a radical change (such as introducing a new material or a new deposition process) is so great that tremendous efforts are made to extend established technology, and these efforts often succeed. Damascene copper plating, recently considered revolutionary, has now become mainstream. Just how this technology and its enabling equipment will continue to advance, whether by evolutionary or revolutionary means, will be exciting to see. ■

FIG. 6. SEM image of superconformal Cu plating in vias with ALD Ru liner (via diameter 0.18 μm).

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