Substrates for the Next Generation Electronics and Photonics

by Jerzy Ruzyllo

Electronic and photonic devices and systems have developed into a dominant global industry. The ever-present need in this industry, to improve device performance and reduce cost, calls for the continued modifications of silicon as well as III-V compound semiconductor manufacturing technologies. In the former case, since the very beginning of an era of MOSFET-based digital integrated circuits, progress was epitomized by the drive toward reduction of horizontal device geometries needed to assure circuits' increased switching speed and packing density. Those modifications continue to cut across the entire manufacturing sequence. In order to fully benefit from reduced device geometries defined at the front-end-of-the-line, major modifications of the back-end-of-the line processes must follow. Introduction of copper as an interconnect material, the growing number of interconnect levels, use of low-k dielectrics as inter-metal insulators, and a broad acceptance of chemical-mechanical planarization (CMP) in mainstream silicon manufacturing, exemplify this trend. As a result, the overall process of transition from one technology generation to another that is based primarily on device scaling is becoming increasingly expensive and technically complex.

Because of the obvious physical limitations that will eventually come to play, as well as due to the technical challenges and cost associated with continued decrease of device geometries, the avenues that would sustain the progress of Si nanoelectronics, but would not rely solely on device scaling, had to be vigorously explored. As it turned out, much in this regard can be accomplished by the proper engineering of silicon substrate wafers used to make cutting-edge devices and by increasing the diameter of Si substrate wafers beyond the current 300 mm. For instance, by using the SOI (silicon-on-insulator) substrates with strain introduced in the active Si layer, not only improved circuit performance can be accomplished without geometry scaling, but also management of heat dissipated during circuit operation is much easier than in the case of bulk substrates.

From the electronic functions' point of view, the III-V semiconductors distinguish themselves from silicon by generally higher electron mobility, while from the photonic applications standpoint by featuring predominantly a direct bandgap. Consequently, the areas of applications of III-V based devices differ from those built in silicon emphasizing ultra-high speed of operation on one hand and efficiency of light emission and detection over the spectrum of wavelengths from UV to deep IR on the other. As a result of these differences, the III-V devices feature different designs and different manufacturing needs than their Si counterparts. Hence, the progress in the former case took a different path than in silicon, emphasizing primarily precision in the control of vertical dimensions in the structures such as superlattices and quantum wells. Also, seemingly more aggressive than in the case of silicon technology, exploration of nanostructured materials in mainstream III-V device technology can be discerned.

Acting on behalf of the ECS Electronics and Photonics Division, it is my pleasure to introduce in this issue of *Interface* three feature articles, the contents of which reflect the above trends. The paper by M. Watanabe and S. Kramer is concerned with a very technically challenging, and potentially prohibitively expensive, transition from the current standard Si wafers that are 300 mm in diameter to 450 mm wafers. The paper discusses various aspects of such a transition, which is anticipated within the next six to eight years. The other paper focusing on Si substrates, and authored by C. Mazuré and G. K. Celler, deals with the issues related to the technology of highly engineered Si substrates. A broad range and diversity of issues discussed in this paper is a clear indication of the importance of this aspect of silicon semiconductor science and engineering. Finally, a paper by E. B. Stokes, A. D. Stiff-Roberts, and C. T. Dameron exemplifies trends in III-V device technology regarding integration of novel nanostructured materials with mainstream manufacturing with a goal of improved performance of next generation photoemitters and photodetectors. ■

About the Author

Jerzy Ruzyllo is a Professor of Electrical Engineering and Materials Science and Engineering at the Pennsylvania State University and the Chair of the Electronics and Photonics Division of the Society. Professor Ruzyllo is a Fellow of ECS and the Fellow of IEEE. He may be reached at jruzyllo@psu.edu.