Performance of Double-Gate SOI nMOSFETs (Gate-All-Around) at Low Temperature.

A. Vandooren*, S. Cristoloveanu**, J.P. Colinge* and D. Flandre***

* Department of Electrical and Computer Engineering, University of California, Davis, CA 95616 USA.
** LPCS, ENSERG, BP257, 38016 Grenoble Cedex, France.
*** Microelectronic laboratory, Place du Levant, 3, 1348 Louvain-La-Neuve, Belgium.

Introduction: Double-Gate SOI MOSFET is considered as a strong candidate for low power CMOS applications and for ultimate ultra-short circuits. These devices benefit of tremendous advantages such as increased drain current, ideal subthreshold swing, reduced short channel effect and reduced leakage currents. Double-gate structures already proved their suitability for operation in harsh environments such as radiative environments [1,2] or high temperature [3]. Bulk and SG SOI circuits already revealed a number of significant improvements when operating at very low temperature [4]. This paper evaluates the performance of double-gate SOI transistors down to 77K. The transistor performance of inversion-mode nMOSFETs are presented. Particular attention is paid to major parameters such as carrier mobility, subthreshold slope and threshold voltage variation.

Experiment: The experiment is performed on 1-μm inversion-mode nMOS Gate-All-Around (GAA) FD SOI MOSFETs fabricated using the process described in [5]. The devices have a silicon, gate oxide and buried oxide thickness of 81nm, 30nm and 400nm, respectively and a film doping of 1e18cm⁻³. Measurements are carried out between 77K and 300K.

Results: The threshold voltage evolution for n-channel devices follows the relationship [6]:

\[ V_T = \phi_s + V_B + \frac{\Delta}{2C_\text{ox}} \ln \left( 1 + \frac{\Delta}{\alpha} \right) \]  

where \( \alpha = \frac{q}{kT} \frac{O_x}{8C_\text{ox}} \) and \( \delta = \frac{C_\text{th}}{4C_\text{ox}} \) are process-dependent parameters, \( V_B \) is the flatband voltage. \( \phi_s \) is no longer equal to the strong inversion limit (2\( \theta_s \)) but is also corrected by a term depending on \( \alpha \) and \( \delta \). This term is usually negligible, resulting in a surface potential at threshold lower than 2\( \theta_s \):

\[ \phi_s = 2\theta_s + \frac{kT}{q} \ln \left[ \frac{\frac{\delta}{\left(1 - e^{-\delta}\right)\phi_s}}{1 + \frac{\Delta}{\alpha}} \right] \]  

These correcting factors take into account weak volume inversion mechanism present in the middle of the silicon film of double-gate structures [7]. The experimental threshold voltage is extracted using the TC method and compared to the above model neglecting and not neglecting the correcting factors \( \alpha \) and \( \delta \). The temperature dependence of interface traps is taken into account by introducing a hyperbolic cosine function of interface trap density distribution in the bandgap. We show that the threshold voltage variation with temperature is independent on the \( E_F(T) \) in double-gate devices. The subthreshold slope in GAA devices is ideal:

\[ S = \frac{kT}{q} \ln(10) \left( 1 + \frac{\phi_s}{C_\text{ox}} \right) \]  

where \( D_i \) is the interface trap density. Assuming a uniform interface trap density in the bandgap, the subthreshold slope varies linearly with temperature with a slope ranging between 0.212mV/dec/K and 0.226mV/dec/K for \( D_i = 5e18 \text{cm}^{-2}\text{eV} \) and 1e19\text{cm}^{-2}\text{eV} respectively. The experimental subthreshold slope variation with temperature is equal to 0.191mV/dec/K and does not show as much improvement as theoretically predicted. This may be due to a temperature dependence of to the effective density of interface traps with temperature. Nevertheless, the subthreshold slope for nMOS transistors shows great improvement from 62mV/dec at room temperature down to 20mV/dec at 77K.

The field-effect mobility \( \mu_{FE} \) is obtained after normalizing the transconductance, \( g_{m} \) by a factor \( C_{ox}(W/L)V_{dd} \). The empirical law for mobility in strong inversion is given by:

\[ \mu_{FE} = \frac{\mu_{FE}}{\mu_0} \]  

where \( \mu_0 \) is the pure mobility and \( \theta \) is the attenuation factor. The method for extracting the effective mobility is based on the computation of the drain current and square root of the transconductance ratio \( L/(2g_0)^{\frac{3}{2}} \). The maximum mobility \( \mu_0 \) is then determined from the slope while the horizontal intercept also provides another definition of the threshold voltage. This procedure is free from series-resistance effects. The attenuation factor and the series resistance are also extracted at low temperature.

Conclusion: We have demonstrated that the Double-gate SOI technology shows great potential for operation at low temperature. They exhibit excellent mobility already at 77K, smaller threshold voltage variation than the bulk or PD SOI transistors and very low subthreshold swing.

References: