P- and *N*- channel Silicon-Germanium Power MOSFETs for Space Systems

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INTRODUCTION

Work has been done to produce III-V semiconductor based heterojunction power MOSFETs. However silicon-germanium power MOSFETs utilizing strained SiGe and Si channels also have the potential for superior performance, especially at low temperatures. Strained SiGe on unstrained Si results in the formation of a potential well in the valence band, where holes accumulate (as a 2DHG) as gate voltage is increased. The mobility of the holes in the well is higher due to reduced interface scattering and lower effective mass. Strained Si on unstrained SiGe yields the opposite – a well in the conduction band, where a 2DEG can form. [1, 2, 3]

This paper reports on the design and fabrication of 1mm to 2 mm wide and 2 to 10 μm long power MOSFETs using SiGe technology for space-borne cryogenic power system applications.

DESIGN

Multiple-finger power MOSFETs of gate lengths from 3, 5, 8 and 10 microns and widths of 1 or 2 mm were designed. The mask layout was made in AutoCAD and 4" chrome on glass masks were fabricated. Other test structures included were van der Pauw structures (for sheet resistance), capacitors (for C-V), diodes (for temperature indication), structures for metal and contact resistance and regular small signal MOSFETs of same gate lengths. Thus the smallest gate length is 3 μm.

Simulation of the SiGe heterostructures was done to find if a certain structure was viable or not and also to compare the performance of the structures. A modified version of the 1-D Poisson solver program by Prof. Gregory L. Snider (Notre Dame) was used to perform the simulations. The program plots the energy level vs. depth, across multiple layers of the heterostructure. The simulation was done for varying gate biases and different temperatures. One p- and one n-channel heterostructure was selected for growth and are shown in Fig 1. The layer thicknesses were chosen to maximize transconductance and to allow as high a processing temperature as possible.

FABRICATION AND CHARACTERIZATION

The strained layers of Si or SiGe that have been epitaxially grown on Si tend to relax if the temperature exceeds the critical value for a certain layer thickness. Also, Ge tends to diffuse at high temperatures. To maintain the integrity of the structure throughout the processing, one cannot use typical high temperature processes. Hence, low temperature processes were developed for gate oxidation and diffusion. The gate oxide was characterised by high frequency C-V measurements performed with an HP4275A LCR meter.

The structures were grown epitaxially by MBE on 1-2 and 38-60 ohm-cm Si <100> substrates. For the p-MOS structure, 1 μm of Si was grown, followed by 100 Å of $Si_{0.7}Ge_{0.3}$ (the channel layer), followed by a 100 Å Si cap layer. For the n-MOS structure, 4.5 μm of SiGe were grown, with the Ge concentration graded from 1.8% to 29.4%. The doping in the graded layer was nominally $3x10^{17}$ cm^{-3} p type. Next, a 1μm thick layer of $Si_{0.7}Ge_{0.3}$ was grown, doped to $1x10^{18}$ cm^{-3} p-type. Together, these layers formed the virtual substrate. Next, a strained Si channel layer, a SiGe layer and a Si cap layer were grown. The wafers were rotated at 15 rpm during the growth. The pressure during the growth was $4x10^{9}$ Torr and the temperature was 500 °C. The background doping of the system is of the order of 10^{16} cm^{-3}, n-type.

Fabrication was started by depositing 5000 Å of field oxide with a Technics PEIIA Plasma System at 450 °C. Source and drain regions were then opened lithographically and spin-on dopant was applied. Phosphorus glass was used for the n-device and boron for the p-device. Diffusion and gate oxide growth were carried out at reduced temperature (730 °C). This was followed by Al metallization and sintering at 450 °C.

Detailed material and electrical characterization will be presented.

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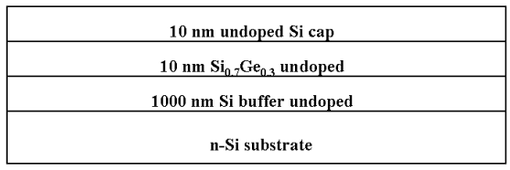
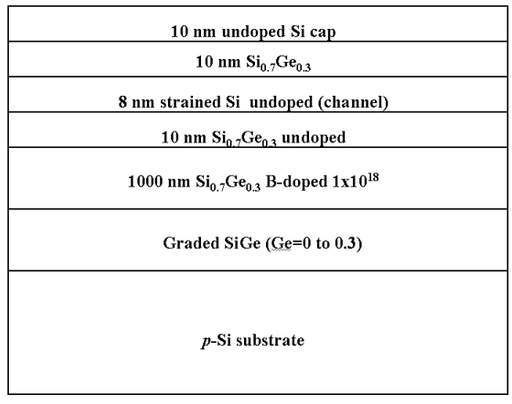


p-channel



n-channel

Fig. 1

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