The effect of HNO_3/HF-last cleanings on the MOS Gate oxide integrity

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The control of the microroughness of silicon wafers has become crucial for obtaining high-quality thin gate oxides in order to manufacture giga scale integration (GSI) circuits.[1,2] Special attention has been given to the effect of pre-oxidation cleaning procedures on the final topography of the Si-SiO_2 interface.[1] Nowadays, it is of fundamental importance the development of pre-oxidation cleaning strategies in order to control the surface topography. A higher performance could be achieved by reducing the metallic and organic contamination without increasing the surface microroughness.[3,4] In this work, it was investigated the effect of HNO_3/HF-last cleanings on the MOS gate oxide integrity.

For all experiments, p-type CZ (Czochralski-grown) (100) wafers, 3 inches in diameter, boron doped, with resistivity in the range of 10 to 20 Ωcm were used. The as-received wafers were submitted to different cleaning procedures with different HNO_3/HF-last steps as follows: ***(a)*** 5HNO_3 (63%): 1HF (49%): 20H_2O; ***(b)*** 2HNO_3 (63%) : 1HF (49%): 20H_2O; ***(c)*** 1HNO_3 (63%) : 1HF (49%) : 20H_2O; ***(d)*** 0.25HNO_3 (63%) : 1HF : 20H_2O; ***(e)*** 40H_2O:1HF; ***(f)*** RCA[4] + 0.25HNO_3 : 1HF : 20H_2O and ***(g)*** RCA[4] + 40H_2O:1HF. After that, each sample was immediately analyzed by AFM (Atomic Force Microscopy). It was observed that the samples, which were cleaned with the aid of the procedures ***d*** or ***f***, presented the lowest average microroughness(≈ 0.040nm) compared to the samples which underwent HF-last steps (≈ 0.055 nm), i.e., cleaning procedures ***e*** or ***g***.

After a given cleaning procedure, the samples were oxidized in a clean furnace under ultra pure O_2 flux at 900°C. Two different oxidation times were used: 90 minutes (denoted by 90) and 25 minutes (denoted by 25) corresponding to approximately 22nm and 11nm, respectively. Following, the samples were immersed in a very diluted HF solution to remove the grown oxide and then access the wafer surface (silicon/oxide interface). The average microroughness substantially increased compared to the non-oxidized samples and the lowest value among the samples (which were oxidized and had the oxide removed) was 0.168 nm for the HNO_3/HF-last cleanings.

MOS capacitors were manufactured having ***f*** or ***g*** as pre-oxidation cleaning recipes and the gate oxide recipe was the same as described above: 90 or 25. Thus, the wafers were named as *f*-90, *f*-25, *g*-90 and *g*-25 in order to indicate the type of cleaning and the oxidation recipe for each one, respectively. After that, it was performed polysilicon deposition, polysilicon doping, aluminum deposition, plasma etching and lithograph to define the MOS capacitors. CxV characteristics of capacitors with area of 9×10^{-4} cm^2 (*f*-90, *f*-25, *g*-90 and *g*-25) were analyzed and low average effective charge ($<5\times10^{10} cm^{-2}$) and low interface trap level density for all the oxides were obtained. In addition, capacitors with area of 1×10^{-2} cm^2 were stressed up to the dielectric breakdown and the yield histograms were constructed. Figures 1 and 2 illustrate the oxide breakdown-field histograms for *f*-90 and *g*-90.

In conclusion, the MOS capacitors produced by using the pre-oxidation cleaning procedure ***f*** presented the highest yield. The mechanism by which the HNO_3/HF-last step can induce metal and particulate removal is based on slight silicon wet etching. Nitric acid (HNO_3) tends to oxidize the surface while the hydrofluoric acid (HF) removes the grown oxide. For the cleaning procedure ***f***, a lower concentration of HNO_3 was used, so that, the HNO_3/HF-last dip promoted a better efficiency of metal/particulate removal and a decrease of the surface microroughness.

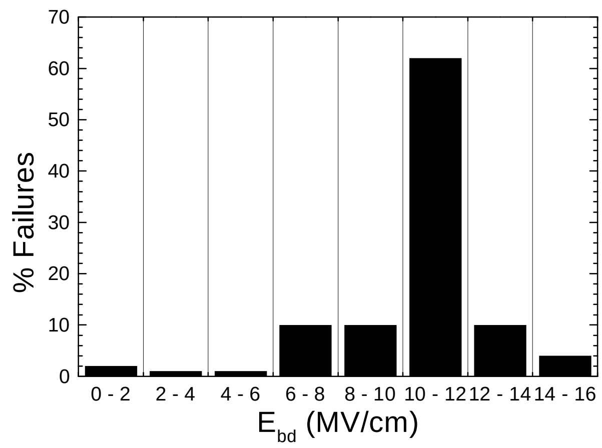

Figure 1 – Typical dielectric breakdown field (E_{bd}) distribution (100 capacitors – gate area of 10^{-2} cm^2) for sample *f*-90 (cleaning recipe *f* and oxidation time of 90 minutes).

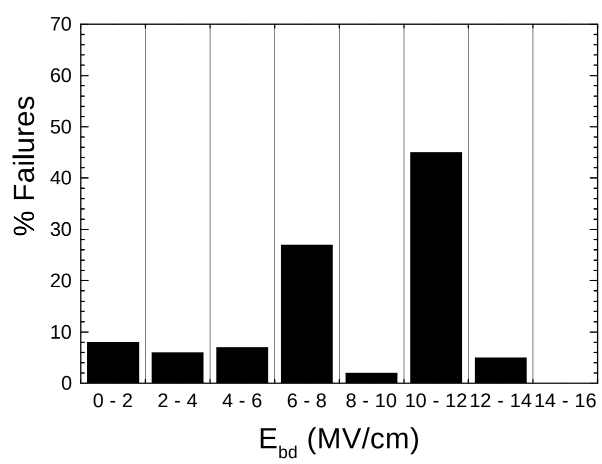

Figure 2 – Typical dielectric breakdown field (E_{bd}) distribution (100 capacitors – gate area of 10^{-2} cm^2) for sample *g*-90 (cleaning recipe *g* and oxidation time of 90 minutes).

Acknowledgement

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References