The breakdown voltage characteristics of Trench High Voltage LDMOS using SOI

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Intelligent power intergrated circuits have become increasingly popular for implementation of system functions with improved performance, reduced size and lower cost. The flat panel display industry has made effective use of power ICs to offer improved features in such areas. Especially the plasma display panel requires the power devices of which breakdown voltage is above 100V(in data driver IC) or 250V(in sustain driver IC). The LDMOS structure is the most used devices in these circuits. In the case of LDMOS, the use of fine lithographies cannot reduce the size imposed by the drift region as the breakdown voltage of the LDMOS is a function of the doping and length of the drift zone. In order to reduce the surface electric field at the end of the gate plate some structure has been proposed. [1]~[3].

In this paper, we proposed a new structure to reduce the electric field at the end of the gate plate, and investigated the breakdown voltage characteristics.

In this work we used the SOI structure. The thickness of the buried oxide is 3um, and the thickness of the p-epi is 8um. And as seen in Fig. 1 we proposed a new LDMOS structure having trench under the gate to reduce the electric field at the end of the gate. We investigated the influence of the drift length, trench depth, trench width and gate length on the breakdown voltage.

Fig. 2 shows the influence of the drift region length on the breakdown voltage in Trench LDMOS structure. As the drift region length increases, the breakdown voltage of Trench LDMOS increases. The breakdown voltage is proportional to the drift region length. When the drift region length is 21um, the breakdown voltage is 280V. So we fixed the drift region length at 21um. Fig. 3 shows the influence of the trench depth on the breakdown voltage. In this case as the trench depth increases the breakdown voltage increase. In this case, we can result that the electric field under the end of gate is reduced. Fig. 4 shows the influence of the trench width on the breakdown voltage. The breakdown voltage increases as the trench width decreases. And Fig. 5 shows the influence of the gate length on the breakdown voltage. When the gate length increases the breakdown voltage decreases.

We proposed a new structure of high voltage LDMOS using SOI and trench structure to improve breakdown voltage characteristics by reducing the electric field under the end of the gate. We could get the higher breakdown voltage by increasing drift region length and trench depth. On the other hand we could get the higher breakdown voltage by reducing the trench width and gate length.

References

[1] D. Lin, S. Larry Tu, Y. See, P. Tam, ”A novel LDMOS structure with a step gate oxide”, IEEE IEDM, 1995, pp. 963-966.

[2] O. Kwon, T. Efland, Wai. T. Ng, ”Optimized 60V lateral DMOS devices for VLSI power Applications”, VLSI Technology Symposium, 1991, pp. 115-116.

[3] A. Nezar, “Breakdown voltage in LDMOS transistor using internal field rings”, IEEE Transactions on Electron Devices. Vol. 38. No. 7 July 1991.

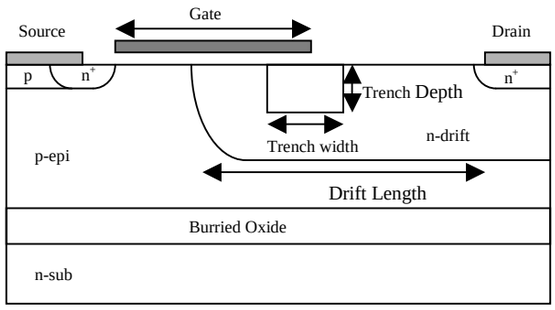

Fig. 1. The structure of proposed Trench LDMOS

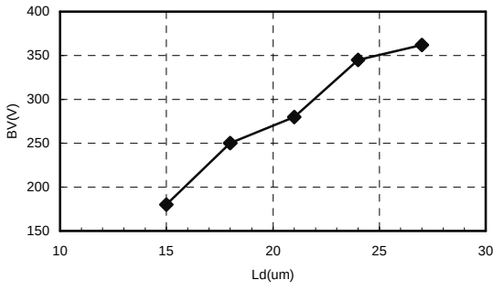

Fig. 2. Breakdown voltage vs. drift region length

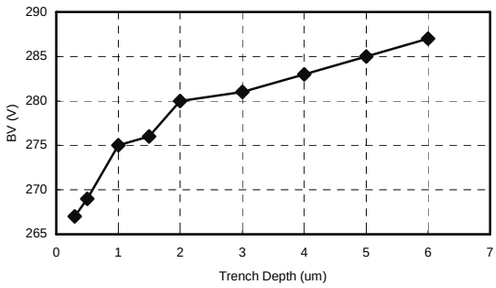

Fig. 3. Breakdown voltage vs. trench depth

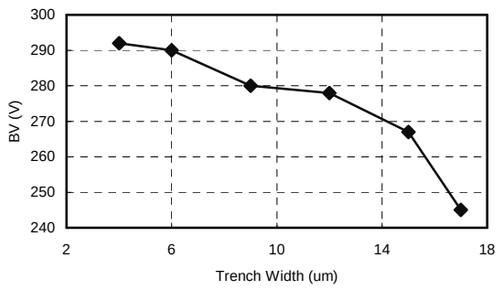

Fig. 4. Breakdown voltage vs. trench width

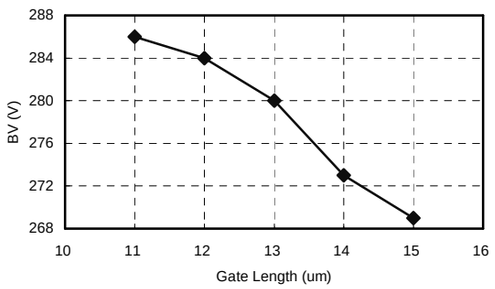

Fig. 5. Breakdown voltage vs. gate length