Impact of Interface Nitridation and Remote-Plasma-Assisted Oxidation (RPAO) Thickness on Breakdown Phenomena and Reliability of Stacked Oxide/Nitride and Oxynitride Dielectrics under Constant Voltage Stress (CVS)

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ABSTRACT

Soft and hard breakdown (SBD and HBD) characteristics of sub-2nm stacked Oxide/Nitride and Oxide/$(SiO_2)_{0.5}(Si_3N_4)_{0.5}$ gate dielectrics prepared by RPECVD are investigated using a constant voltage stress (CVS) under inversion mode. Gate current fluctuation with increasing stress time is observed after the appearance of soft breakdown (SBD); multilevel SBD is observed in thermal oxide, and only O/N dielectric without interface nitridation shows HBD events (Fig. 1). The O/N dielectric without interface nitridation reveals increased tunneling current, off-state drain current (Fig. 2), more negative V_t shifts and degraded electrical characteristics after CVS, indicating a significant reduction of hole trapping in the gate-to-drain overlap region. A strong area dependence of oxide breakdown is observed. Experimental evidence shows enhanced early breakdown and significant degradation on device parameters such as V_t shift, $I_{d,sat}$ and maximum transconductance (g_m) for small-area MOSFETs. An increased stress-induced leakage current (SILC) is also observed in short-length devices attributed to higher probability of overlap of two neighboring traps which results in the formation of a low-resistive conducting path. The drain current is degraded in the saturation region, and at higher gate voltages above 2.2V, a positive drain current is observed due to a significant increase in hole current from drain to gate (Fig. 3). In addition, the effect of remote-plasma-assisted oxidation (RPAO) thickness on device breakdown of oxynitride dielectrics is studied. For both PMOS and NMOS capacitors, stacked oxide/oxynitride dielectrics with 0.6nm RPAO show higher charge-to-breakdown (Q_{BD}) and TDDB reliability compared to the dielectrics with 0.8nm RPAO. It is observed that thicker RPAO shows multilevel early SBD due to a larger number of broken H-O and Si-H bonds and strained Si-O bonds generated in the buffer oxide layer during CVS; however, similar breakdown mechanism is observed due to the identical TDDB slope (Fig. 4).

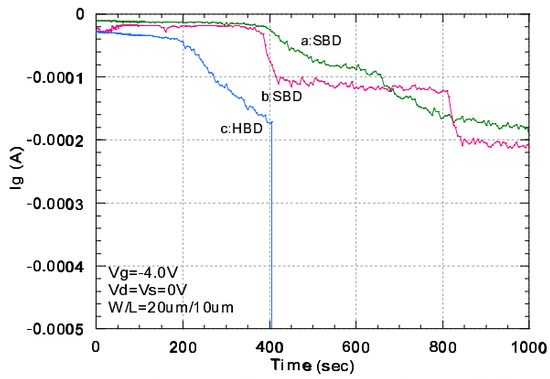

Fig.1 SBD and HBD characteristics of gate dielectrics under CVS. a: O/N with interface nitridation; b: thermal oxide; c: O/N without nitridation.

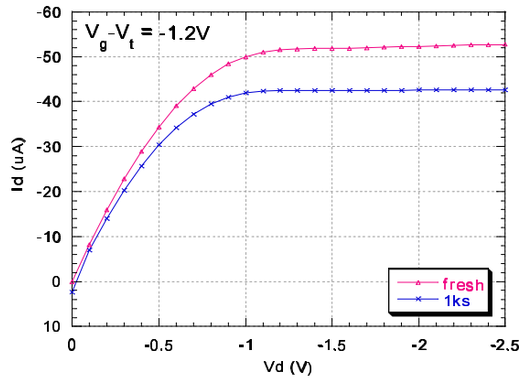

Fig.2 O/N dielectric without nitridation shows a positive drain current at Vd=0V after CVS for 1k sec, indicating a significant hole trapping at Si/SiO_2 and junction interfaces.

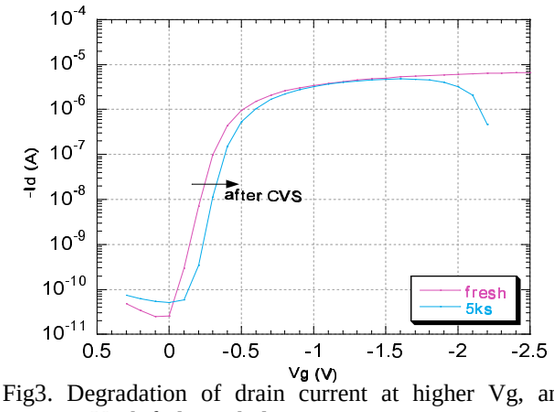

Fig3. Degradation of drain current at higher Vg, and negative Vt shift due to hole trapping.

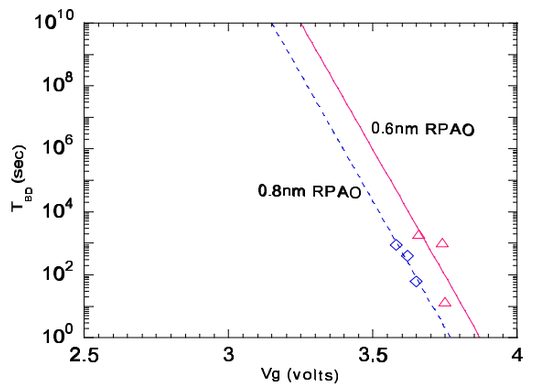

Fig.4 Effect of RPAO thickness on TDDB for PMOS with oxynitride dielectrics.