Electrical Characterization Techniques for Semiconductors and Semiconductor-Dielectric Interfaces - A Review

M.J. Deen
Electrical and Computer Engineering, CRL 226
McMaster University, Hamilton
Ontario, Canada L8S 4K1
E-mail: jamal@mcmaster.ca

In recent years, there has been tremendous interest in electrical characterization techniques for dielectric-semiconductor interfaces and to relate the results of these measurements to the reliability of the device or component. Further, most investigators prefer to use techniques that do not require special test structures, but rather to use techniques that can be easily and readily applied to standard test structures routinely manufactured for process file development, for example. This review will discuss the following important techniques which have seen much use in recent years in probing the characteristics of semiconductors and semiconductor-dielectric interfaces, especially the silicon-silicon dioxide interface and the channel of MOS transistors.

- Low frequency noise as a tool to probe microscopic transport characteristics in semiconductors and bulk and interfacial defects [1-7].
- Charge pumping to probe spatially the distribution of fast interface defects near the channel edges of a MOS transistor [8].
- Floating gate to measure the MOS transistor's gate leakage down to and below the femtoamperes of current level [9-11].
- Simple forward and reverse current-voltage measurements to probe the properties of the source and drain ends of MOS transistors as well as its channel and the channel-gate dielectric interface before and after hot-carrier stressing [10,11].
- Constant resistance deep-level transient spectroscopy to probe electrically active point defects that are responsible for the creation of deep levels in the semiconductor bandgap, and to distinguish between bulk and interfacial defects in MOS transistors [12,13].

In this paper we will carefully review the above electrical characterization techniques, point out their advantages and limitations, and also discuss areas of future research. In addition, we will indicate how the device measurements are related to the performance of devices [14,15] and circuits made using both silicon as well as compound semiconductor technology [5,6]. Finally, we will explore the connection between results from these electrical measurements and the reliability of devices and circuits using representative circuits such as oscillators or low noise amplifiers.

References

1. M.J. Deen, M.E. Levinshtein, S.L. Rumyantsev and J. Orchard-Webb, *Generation-Recombination Noise in MOSFETs*, **Semicond. Sci. Tech.**, Vol. 14(3), pp. 298-304 (March 1999).
2. M.J. Deen, S.L. Rumyantsev and M. Schroter, *On the Origin of 1/f Noise in Polysilicon Emitter Bipolar Transistors*, **J. App. Phys.**, Vol. 85, pp. 1192-95 (Jan. 1999).
3. M.J. Deen, O. Marinov, J. Yu, S. Holdcroft & W. Woods, *Low Frequency Noise in Polymer Transistors*, **IEEE Trans El Dev.**, Vol. 48, pp. 1688-95 (Aug. 2001).
4. M.J. Deen, S.L. Rumyantsev, D. Landheer & D.-X. Xu, *Low Frequency Noise in Cadmium Selenide Thin-Film Transistors*, **App. Phys. Lett.**, Vol. 77, pp. 2234-36 (2 October 2000).
5. S. An and M.J. Deen, *Low Frequency Noise in Single Growth Planar Separate Absorption, Grading, Charge and Multiplication Avalanche Photodiodes*, **IEEE Trans. El. Dev.**, Vol. 47, pp. 537-43 (March 2000).
6. S. An, M.J. Deen, A.S. Vetter, W.R. Clark, J.-P. Noel & F.R. Shepherd, *Effect of Mesa Overgrowth on Low-Frequency Noise in Planar Separate Absorption, Grading, Charge and Multiplication Avalanche Photodiodes*, **IEEE J. Quantum Elec.**, Vol. 35, 1196-1202 (Aug. 1999).
7. M.J. Deen, *Low Frequency Noise as a Characterization Tool in InP and GaAs-Based Double Barrier Resonant Tunneling Diodes*, **Mat. Sci. Eng. B**, Vol B20, pp. 207-13 (1993).
8. X.M. Li and M.J. Deen, *Determination of the Interface State Density in MOSFETs Using the Spatial Profiling Charge Pumping Technique*, **Solid-State Electronics**, Vol 35, pp. 1059-63 (Aug. 1992).
9. A. Raychaudhuri, M.J. Deen, M.I.H. King and W. Kwan, *A Simple Method to Qualify the LDD Structure Against the Early Mode of Hot-Carrier Degradation*, **IEEE Trans. El. Dev.,** Vol 43), pp. 110-15 (Jan. 1996).
10. A. Raychaudhuri, M.J. Deen, M.I.H. King and W. Kwan, *Features and Mechanisms of the Saturating Hot-Carrier Degradation in LDD MOSFETs*, **IEEE Trans. El. Dev.,** Vol 43, pp. 1114-22 (July 1996).
11. W.S. Kwan, A. Raychaudhuri and M.J. Deen, *Location and Quantification of the Interface Defects in Stressed MOSFETs Using a Combination of Floating Gate and Transconductance Techniques, and Charge Pumping Methods*, **Canadian J. Phys. (Special Issue for CSTC 1995)**, Vol. 74, pp. S167-S171 (1996)
12. P. Kolev and M.J. Deen, *"Development and Applications of a New DLTS Method and New Averaging Techniques"*, **Advances in Imaging & Electron Physics,** Ed. P. Hawkes, Academic Press, New York, Vol. 109, pp. 1-161 (1999).
13. P. Kolev, M. J. Deen, T. Hardy and R. Murowinski, *A New Voltage Transient Technique for Deep Level Studies in Depletion-Mode Field-Effect Transistors*, **J. Electrochem. Soc.**, Vol. 145(9), pp. 3258-64 (Sept. 1998).
14. W.S. Kwan, C.H. Chen and M.J. Deen, *Hot-Carrier Effects on RF Noise Characteristics of LDD MOSFETs*, **J. Vacuum Sci. Tech. (Special Issue for CSTC 1999)**, Vol. A18(2), pp. 765-69 (March/April 2000).
15. W.S. Kwan and M.J. Deen, *Hot-Carrier Effects on the Scattering Parameters of LDD MOSFETs*, **J. Vacuum Sci. Tech. (Special Issue for CSTC 1997)**, Vol. A16(2), pp. 855-59 (March/April 1998).