Thickness Scaling of Gate Dielectric on Plasma Charging Damage in MOS Devices

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Since the thickness of conventional thermal oxide is intrinsically limited, other alternative gate dielectrics with high dielectric constants (k), which are physically thicker while electrically equivalent to ultra-thin thermal oxide, must be considered. Si_3N_4 and Ta_2O_5 appear to be most favorable due to plenty of researches demonstrated [1, 2]. Plasma processes are widely employed to transfer the shrinking feature size successfully for the fabrication technology of ULSI devices. However, the plasma process induced charging damage was found to degrade the electric characteristic and reliability of gate dielectric [3, 4]. Thus plasma process induced charging damage on high-k gate dielectrics deserves to explore as it is rarely reported. Scaling effects of gate dielectric thickness on plasma process induced charging damage in MOS devices is particularly investigated in this work.

Gate oxides with thicknesses of 2.5 and 4.0 nm were formed in dry O_2 by a thermal furnace. Si_3N_4 dielectric was deposited in NH_3 at 800 ℃ and in NH_3/SiH_2Cl_2 at 720 ℃ in sequence by LPCVD and then rapid-thermal-annealed in N_2O at 850 ℃ and 800 ℃ for 15 sec, respectively. Ta_2O_5 dielectric was reactively sputtered and then plasma-annealed in N_2O for 60 sec and finally rapid-thermal-annealed in N_2 at 600 ℃ for 30 sec. Gate dielectric physical thickness was measured by ellipsometry. Equivalent oxide thicknesses (EOT) were 2.8 nm for Si_3N_4 film (k=5.4) represented by sample N and 3.0 / 3.2 nm for Ta_2O_5 film (k=26.8) represented by samples T1/T2, as determined by capacitance-voltage method. The physical thickness difference between sample T1 and T2 is 2.0 nm. The interfacial oxynitrides for sample N and T1/T2 are 1.27 and 1.69 nm, respectively. A set of antenna structures with edge-intensive patterns was applied to investigate the plasma charging damage. Different antenna periphery length (AL) from 4 to 320 mm with the same antenna ratio (AR= 10 k) was designed.

The hot carrier stress induced electrical degradation for MOS transistors with various gate oxide thicknesses is shown in Figure 1. The degradation of transconductance and drain current along AL is obvious for the MOS transistors with 4.0 nm gate oxides. However, MOS devices with ultra thin gate oxide (2.5 nm) hardly suffer from plasma charging damage as AL is increased. This might be attributed to the conduction mechanism of plasma charging current converted from Fowler-Norheim tunneling to direct tunneling. Thus, the electrical property degradation induced by plasma charging damage may be slight as gate oxide thickness scales down.

Figure 2 shows time to breakdown (Tbd) for MOS devices with high-k gate dielectrics at various effective electrical fields represented by E-model. Devices with Ta_2O_5 film have apparently larger Tbd than those with Si_3N_4 film, which may be due to the larger physical thickness for Ta_2O_5 samples. Although the degradation for sample N is the smallest, its time to breakdown is relatively short as compared to that for sample T1 or T2. Regarding to the thickness effect of Ta_2O_5 film, a thicker film clearly reveals a considerable trap-related reliability problem. The trap-assisted tunneling mechanism makes a thicker physical thickness of Ta_2O_5 film, a trap-richer dielectric [5], more susceptible to plasma charging induced damage.

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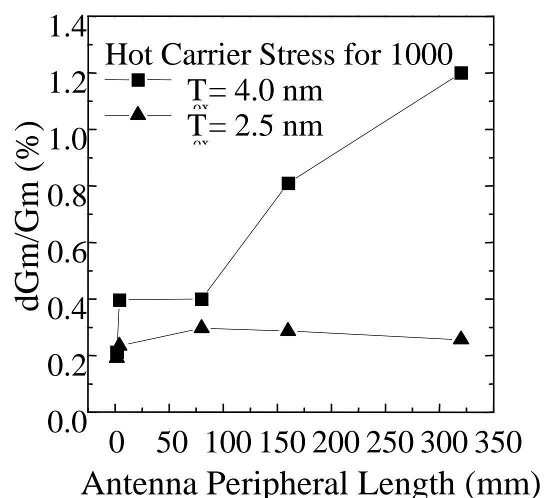

Figure 1 Scaling Effect of gate oxide thickness on the degradation of transconductance for MOS transistors after hot carrier stress for 1000 sec.

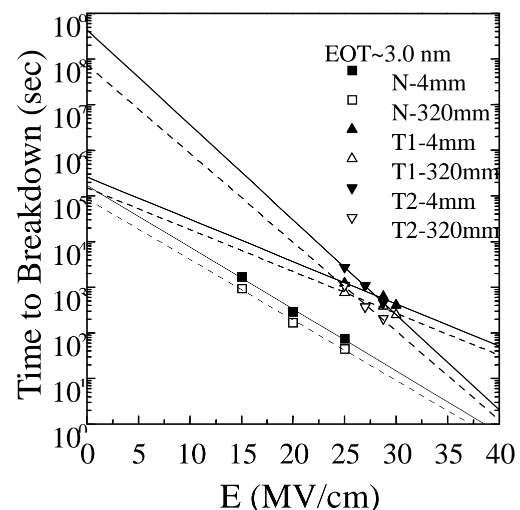

Figure 2 Time-to-breakdown Tbd of MOS capacitors with high-k gate dielectrics under various effective electrical fields represented by E-model