GATE OXIDE INTEGRITY AND MICROLOADING CHARACTERIZATION OF 300mm PROCESS TOOLS

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Introduction

This paper will discuss characterizations on gate oxide integrity from 300mm diffusion furnaces and microloading effects on 300mm Etch and CMP tools, with process technology development and equipment improvements including experimental data and results from SEMICONDUCTOR**300** (a joint venture between Motorola, Inc. and Infineon Technologies through September 2000).

Experimental

300mm Epi wafers were used for the gate oxide integrity study. The Etch 300mm test wafers consisted of a 45nm SiN ARC layer on 800nm of BPSG annealed over silicon, and imaged with a DRAM or logic pattern. The CMP 300mm test wafer construction consisted of 800nm BPSG-annealed oxide film overlying a patterned 165nm TEOS oxide film, covered with a 5.5nm liner nitride film to serve as a delineation layer during cross-sectional analysis, or overlying a 200nm Cap nitride layer patterned with the logic pattern.

Results and Discussion

The purpose of this characterization was to gain an understanding of the gate oxide integrity (GOI) differences on wafers processed in the 300mm furnaces at SEMICONDUCTOR**300** (SC300 – joint venture between Motorola and Infineon Technologies), compared to similarly processed 200mm wafers, in a sister factory. Comparing gate film quality and GOI data between different facilities can be difficult. Primarily differences in chemicals, processes, tooling and sampling are important, and must be accounted for in the data. Measurement techniques cannot easily discriminate between the individual charge components, so total oxide charge is often monitored. Mercury probing was a technique that was used to measure the amount of charge contained in the oxide. The GOI measured values were considered to be within an acceptable range between the 300mm and 200mm wafer furnaces. The main difference observed was a large and increasing hysteresis behavior on successive wafer runs.

Separately, an investigation was done on incoming particle contamination levels on the 300mm Epi wafers used for this study. Contamination occurred in various forms on the wafer and caused unintentional changes in electrical properties of the semiconductor devices. To prevent contamination from affecting device performance, up to 25% of all wafer manufacture processing consists of cleaning steps. From a device standpoint, the amount of electrically-active impurities in oxides must be minimized because embedded impurities attract or repel free charges in the underlying silicon. In most cases, device performance depends strongly on the concentration of free charges in the silicon. Variations in oxide contamination usually introduce unwanted variations in device performance.

A project to investigate microloading effects on the Etch and CMP polish processes was undertaken to identify process sensitivities and interactions with these operations. This investigation was done by obtaining data on the microloading effects from the 300mm Oxide etch and CMP polish tools and processes, primarily used for DRAM manufacturing at SC300. Microloading effects impact various process outputs including non-uniformity on both processes, etch depth on Etch processes, and dishing/cusping defects on CMP processes. Etch rate uniformity variation from the wafer's center to edge tend to magnify the microloading effects, and contact/via features tend to be most susceptible to these effects. CMP microloading can impact dense and isolated features, and together with process non-uniformity, are a critical concern on 300mm tools and processes. Three different sets of wafers were built to study these process effects. These included oxide test wafers for Etch studies, and two sets of CMP wafers to study oxide and nitride film polish effects. SEM micrograph cross-sectional analysis was used to obtain the data. The data showed that the standard Etch process resulted in significant microloading effects between the contact holes and interconnect features. The etch rate loss difference was reduced significantly by adjusting the etch process parameters. For the CMP analysis, an inspection was done on isolated linewidth features where the polish stopped on the nitride film. Some observable oxide dishing or significant erosion of the nitride lines was observed. On dense linewidths, oxide dishing was also variable. The film planarity above the nitride and oxide surfaces was similar. Normally, non-optimized CMP processes would produce some dishing in the oxide film and erosion on the exposed nitride surfaces. Comparing the results from the 200mm and 300mm CMP systems indicated that there were only small differences in planarity or microloading between the comparable tools and processes. Adjustment to the CMP processes was done to minimize these negative effects and match the 200mm tool outputs.

Conclusion

The GOI measured values were considered to be within an acceptable range. The Etch process characterization showed significant microloading effects between the contact holes and interconnect features. The CMP analysis indicated that there was only a small difference in planarity and microloading between the 300mm and 200mm wafer comparable tools and processes.

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References

1. K. Mautz, *Plasma Etching Processes for 0.25u Device*s, **99-30**, 1 (1999).
2. K. Mautz, *10th Symp. Plasma Process Proc.*, **98-4**, 242 (1998).
3. B. Johnson et al., *Future Fab*, **1,** 3 (1997).
4. C. Haris et al., *Future Fab***, 7**, 59 (1999).