ETCHING OF HIGH K GATE DIELECTRIC AND GATE METAL ELECTRODE CANDIDATES

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INTRODUCTION

High K gate dielectrics and metal gates are being widely studied for next generation devices, especially for low-power applications. Use of these new materials impose new integration problems, including selective etching of the high K gate dielectrics and the metal gate electrodes. First it is necessary to etch gate metal for NMOS and PMOS devices, stopping on the high K dielectric. In some cases the gate electrode may be composed of two layers of metal, e.g. W on Ru. Then it is necessary to etch the high K dielectric or an SiO_2/high K laminate and stop on silicon. This paper reports reactive ion etching (RIE) and wet etching of various high K dielectrics and gate electrode materials.

EXPERIMENTAL

All the etching experiments presented in this paper were part an actual device fabrication process. The non-self aligned gate process has been used to fabricate devices having a variety of high K gate dielectrics and gate metals. Two different RIE systems were used to dry etch the gate stacks; 100TP (SEMI GROUP) and SLR720 (PLASMA THERM). Both 100TP and SLR720 systems use parallel plate electrodes with 13.56 MHz radio frequency (rf) power to generate plasma and have a cathode area of 324 cm^2 and 248cm^2, respectively.

RESULTS AND CONCULSIONS

Etching process and results for different dielectrics and metal electrodes are summarized in Table I and II.

One of the major concerns associated with Pt and TaN wet etching was the limited photoresist stability and adhesion to the substrate. In order to circumvent the adhesion loss, it was necessary to periodically re-bake the photoresist at 115 °C for every 10 minutes and 5 min for Pt and TaN, respectively. Oxidation of Pt during the standard photoresist descum was seen to inhibit aqua-regia etching of Pt. To remove this oxide layer and restore normal Pt etching rates, Ar^+ ion milling was performed at 80 Watts, 20 sccm at 60 mtorr for 3 minutes. A critical issue with TaN etching was the variable nitrogen content which influence its resistivity and etch rate.

RIE processes were developed for RuO_2, Ru and W/Ru gate electrodes. Etching of RuO_2 has been shown to occur by O_2 ion assisted etching through the formation of volatile RuO_3 and RuO_4 [1,2]. However O_2 plasma etching has poor selectivity to the photoresist. In order to enhance etch selectivity, a small amount of CHF_3(2.5%) was added. In contrast to RuO_2 etching, the etch rate of Ru electrodes in pure oxygen was negligible. Etch rates as high as 5 nm/min could be obtained by the addition of a few percent Cl_2 to the etch gas. Since this etching rate was considerably slower than that of photoresist, our strategy was to employ a laminated gate of a thin Ru layer (3 nm) covered with a thicker W film (100 nm).

The etching characteristics of high K gate dielectrics depended not only on the materials, but also on the deposition system, substrate pretreatment and post deposition anneal conditions. For instance, jet vapor deposition (JVD) HfO_2 would etched in BOE (10% HF), while all the other HfO_2 films were dry etched. Similarly, rapid thermal CVD (RTCVD) ZrO_2 was dry etched and all the other ZrO_2 films were wet etched in BOE as described in Table II.

Gate Metals	Etching Recipe
Pt (MBE)	Wet etching (H_2O:HCl:HNO_3 = 4:3:1) Temperature: 45 ºC Etching rate: 1.5-2.0 n/min
TaN (PVD)	Wet etching (H_2:HNO_3:HF= 7.35:0.6:2.05) Temperature: 20 ºC Etching rate: 2.7-3.3 n/min
RuO_2 (PVD)	Dry etch: O_2/CHF_3 (20 sccm/0.5 sccm), at 40 mtorr, 150 Watts Etching rate: ~40 nm/min
Ru (PVD)	Dry etch: O_2/Cl_2 (20 sccm/1 sccm), at 15 mtorr, 150 Watts Etching rate: 2~5 nm/min
W(PVD)	W Dry etch: SF_6/O_2 (18 sccm/2 sccm), at 40 mtorr, 150 Watts Etching rate: > 50 nm/min

Table I. Optimized etching recipe for metal gate electrode candidates

Dielectrics	Etching Recipe
HfO_2 (PVD, RTCVD, MOCVD)	Ion milling: Ar (20 sccm), at 15 mtorr, 150 Watts Etching time: 2 min for 5 – 6 nm
HfO_2 (JVD)	Wet etching: BOE (10 %HF) Temperature: 20 ºC Etching rate: 3.5 n/min
ZrO_2 (RTCVD)	Ion milling: Ar (20 sccm), at 15 mtorr, 150 Watts Etching time: 2 min for 5 – 6 nm
ZrO_2 (PVD, MBE, JVD)	Wet etching: BOE (10 %HF) Temperature: 20 ºC Etching rate: 6.0 n/min
La_2O_3 (MBE)	Ion milling: Ar (20 sccm), at 15 mtorr, 150 Watts Etching time: 2 min for 5 – 6 nm
Y_2O_3 (RPECVD)	Wet etching: BOE (10 %HF) Temperature: 20 ºC Etching rate: 6.0 n/min

Table II. Optimized etching recipe for high K gate dielectrics candidates

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