Etching of High Aspect Ratio Silicon Trenches.

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High aspect ratio (AR) trenches are necessary to achieve large values of capacitance in the fabrication of charge storage capacitors in DRAM devices. Etching of high AR trenches suffers from the inherent RIE lag mechanism caused by reduced energy of ions and number of etching species at the bottom of a deep trench. In this paper, two methods are proposed to minimize these problems and thereby achieve significantly higher silicon etch rates and deeper trenches.

The gas mixture used in our work described in this paper is HBr + NF_3 + O_2. The trench etching process is so designed as to deposit a thin passivation film on the sidewalls continuously as the trench is being etched. This oxide-like passivation film ($SiO_xF_yCl_z$) prevents the trench sidewalls from being etched while the surfaces in the XY plane get etched. Balanced formation of the passivation film during etching is critical in being able to achieve high degree of anisotropy in high aspect ratio trench etching. Although the passivation film is formed on all surfaces including the etch front, the film on the trench bottom is continuously removed by the energetic ions that are incident on this surface. The films on the sidewalls however are not bombarded by ions (except those regions that receive ions coming at grazing angles and having energies > threshold energy) and therefore are not etched, thereby preventing lateral etching of silicon. This procedure also leads to increased mask selectivity, since the passivation film is also deposited on the mask surface, decreasing its effective etch rate.

It has been noted that the etching process has a deposition component built in, which builds up an oxide-like passivating film on trench surfaces. Because the walls near the trench opening are exposed longest to the plasma with high concentration of reactants, the deposits here are thicker (> 25 nm) and gradually thin down with depth to < 5 nm. Another reason for thinner deposits in the lower parts of the trench is that some ions deflected from the sloped mask arrive in this region at grazing angles and thin down the film. The direct consequence of thicker deposits at the top is that the opening is constricted, thereby reducing this critical dimension, which in turn increases the RIE lag by reducing the number of ions & neutrals entering the trench hole. Achievable depth is therefore reduced and so is the cell capacitance. It is obvious that periodic enlargement of this opening by thinning the liner will allow more etch species into the trench with increased solid angle at the bottom and therefore achieve higher silicon etch rate.

Although thinning can be done in a separate system, we propose to perform this step in-situ in this paper. This in-situ plasma cleaning process needs to be tailored as to not etch the mask significantly during this step. This is critical because the thinning process, by requirement, will have little or no deposition component in the plasma. We have successfully used a mixture of silanes (e.g. SiH_4) and a F-containing gas (e.g. NF_3) with little or no oxygen for this thinning step.

Another method involves removal of the passivation film at the trench bottom. As discussed earlier, the trench etching process causes the deposition of a blocking film at the bottom surface of the trench, which if not removed results in etch stop. Theoretically, an etch stop occurs when the incoming ions that impinge on this bottom surface do not have adequate energy to activate the chemical etching/removal of the blocking film. Loss of ion energy increases with increase in trench depth due to increased number of inelastic collisions of off-axis ions with the trench walls. Reduction of RIE lag from this mechanism, therefore, requires the removal of this passivation film intermittently at high aspect ratios, using a specially formulated process. This process, as in the previous section, is also strict etching plasma without any built-in deposition component. In addition, the process is operated at much lower pressures to facilitate a larger number of off-axis ions reaching the trench bottom. The experiments show that, by repeating this in-situ plasma cleaning step a few times, the differential silicon etch rate at high aspect ratios is significantly increased. Increase of > 50% silicon etching rates at aspect ratios of > 45 have been achieved, when compared to rates achieved without removing the blocking layer at the trench bottom.