

Patterning 180 nm Copper-Oxide Dual Damascene Baseline with 193nm Resists

Vivek Bakshi and Gregory Smith

Advanced Tool Development Facility,
International SEMATECH, Inc.
2706 Montopolis Drive, Austin TX, USA 78741

At Advanced Tool Development Facility (ATDF) in International SEMATECH, we run baseline lots to monitor the health of the manufacturing line. To monitor the health of back-end line we run 250 nm node copper-oxide dual damascene baseline, which consists among other structures, via chains with 1000 to 1,080,000 vias in series, connected by links designed not to contribute to the total structure resistance. As we transition from 248 nm resists to 193 nm resist for patterning, we are also moving our baseline to 180 nm node [1,2]. In this paper we describe the etch development efforts to pattern 180 nm node copper-oxide dual damascene baseline product, consisting of 170 nm and larger via chains, with 193 nm resists.

The Via First Dual Damascene method is used to form the metallization. In this method, the dielectric stack is formed over M1, consisting of a dielectric barrier (Si3N4), oxide to form the interlevel isolation (400 nm of SiO2, deposited using PECVD in SiH4 and N2O), 75 nm of Si3N4 as an etch stop for Metal 2 etch, and 500 nm of oxide for forming Metal 2. The vias are patterned and etched through the M2 oxide, the M2 etch stop nitride, the interlevel isolation, stopping on the silicon nitride barrier over M1. Fig. 1 shows this with the resist left on. M2 is then patterned using BARC, and etched down to the M2 nitride etch stop. The resist is then removed by ashing in NF3, O2 and forming gas ambient. The final critical etch dry removes the nitride at the bottom of the via, and at the bottom of metal 2. This leaves the wafer ready for barrier and seed metal deposition, plating, annealing, and CMP to form the two level metal structure.

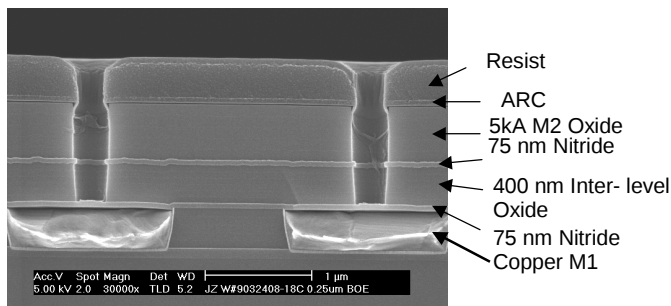


Figure 1: SEM cross-section of 250 nm via for copper dual Damascene with the resist left on. HF stain for layer delineation.

For 248 nm resists, we use C4F8 based high etch rate and high selectivity (to nitride) etch chemistry to pattern 250 nm via chains. The via etch consists of etching of first oxide using high etch rate chemistry, etching of nitride and then etching of lower bottom oxide using a high selectivity etch. In the etching of 193 nm resist, the main challenge for us was the reduced resist thickness; as compared to 7600 Å of 248 nm resist, we had only 3900 Å of 193 nm resist.

Initial experiments showed that high selectivity etch chemistry could not open the bottom vias and the use of high etch rate chemistry for the etching of bottom oxide

gave good via profile. In addition, we had to change our nitride etch to a higher selectivity etch, due to limited resist available for the etch. However, electrical test result showed low yield and drop-off of yield at larger via sizes. Defect inspection showed missing and blown vias but did not give us clues on the reasons for drop of yield at larger via size. We expected NF3 ash, after via etch, to be damaging the larger vias, resulting in yield loss at larger vias. However, SEM showed that there was no punch through of the bottom nitride.

In the next attempt, we added the high selectivity etch to the bottom oxide etch and performed a design of experiment. DOE gave us a model showing the drop of yield at larger via sizes and need to incorporate both high etch and high selectivity etch for the bottom oxide, in order to avoid the yield drop off at larger via sizes. With this new recipe, we have 73% yield at 170 nm and 93% or higher yield at 200 nm and larger vias. [Figure 3] We are performing an optimization DOE to further improve the yield.

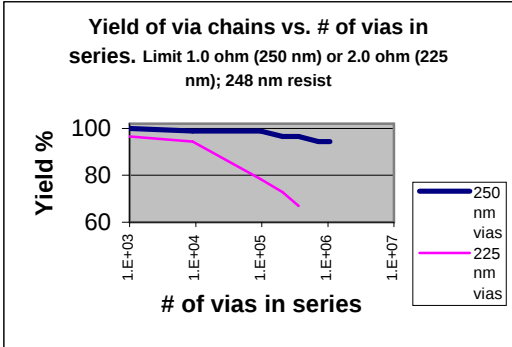


Figure 2: Yield for 250 nm via chains Etch Development

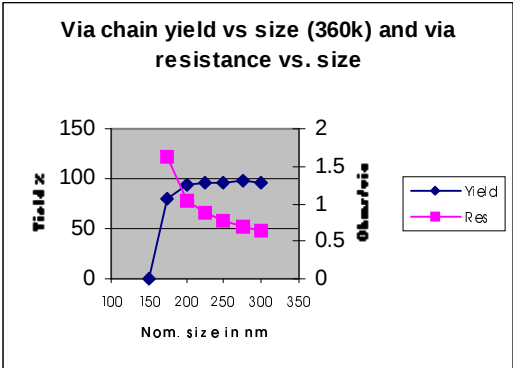


Figure 3: Yield of various via chains, patterned with 193 nm resists

Acknowledgement: We would like to thank from International SEMATECH: Siew Dorris, Spencer Pearson and Gilbert Molina for 193 nm lithography.

References:

[1] **Patterning with 193 nm Resists**, Vivek Bakshi et al *200th Electrochemical Society Meeting*, Session L1A- Thin Film Materials, Process and reliability, September 2, 2001, San Francisco, Ca, USA.
[2] **Status of 193 nm technology**, Vivek Bakshi, James Beach, Sri Satyanarayan, Arnie Ford, *Solid state Technology*, pp. 54, November 2001.