Physical and Predictive Models of Ultra Thin Oxide Reliability in CMOS Devices and Circuits

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The microelectronics industry owes its considerable success largely to the existence of the thermal oxide of silicon. However, recently there is concern that the reliability of ultra-thin dielectrics will limit further scaling to slightly thinner than 2nm. I will review the physics and statistics of dielectric wearout and breakdown in ultra thin SiO_2-based gate dielectrics and discuss the implications of recent long term (>1 year) stress experiments on ultrathin SiO_2 and oxynitride films.

Electrons or holes tunneling through the gate oxide generate defects until a critical density is reached and the oxide breaks down. The critical defect density is explained by the formation of a percolation path of defects across the oxide. Only < 1% of the these paths ultimately lead to destructive breakdown, and the microscopic nature of these defects is not known. The rate of defect generation decreases approximately exponentially with supply voltage, below a threshold voltage of about 5 V for hot-electron-induced hydrogen release. However, the tunnel current also increases exponentially with decreasing oxide thickness, leading to a decreasing time-to-breakdown and a diminishing margin for reliability as device dimensions are scaled. Estimating the reliability of the dielectric requires an extrapolation from the measurement conditions (e.g., higher voltage) to operation conditions. Because of the diminished reliability margin, it has become imperative to try to reduce the error in this extrapolation. Long term (>1 year) stress experiments are now being used to measure the wearout and breakdown of ultra thin (<2 nm) dielectric films as close as possible to operating conditions. These measurements have revealed the details of the voltage dependence of the defect generation rate and critical defect density, allowing better modeling of the voltage dependence of the time-to-breakdown. For long stress duration (days to years) a greater defect density is required to trigger breakdown, contrary to the assumption that the critical defect density should be independent of the stress condition. The defect generation probability exhibits a sigmoidal inflection between 2-3V. Measured over a sufficiently wide range of stress conditions, the time-to-breakdown (T_{BD}) does not obey any simple "law" such as exponential dependence on E, $1/E$, or V_g, as has been commonly assumed in reliability extrapolations. We will discuss the nature of the electrical conduction through a breakdown spot, and the effect of the oxide breakdown on device and circuit performance. In some cases an oxide breakdown may not lead to immediate circuit failure, so more research is needed in order to develop a quantitative methodology for predicting the reliability of circuits.