

SOI Technology: The Future Will Not Scale Down

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Silicon On Insulator (SOI) is usually defined as a young technology for the future of the microelectronics industry. This definition brings three questions:

1. Is SOI really young? Yes, because the past hardly covers 30–35 years only. No, because this is twice longer than what is left on the microelectronics roadmap (ITRS).
2. Is SOI for the future? Yes, bulk-silicon technology cannot make it and there is nothing left but SOI. This answer is reached after careful elimination of potential candidates, not by enthusiasm or generosity for SOI.
3. Is the future still what it used to be? No, SOI allows expanding the frontiers, foreseen and feared, of bulk-Si.

The aim of this paper is to document the above interrogations and answers from the viewpoint of material scientists and device physicists. We briefly trace the past of SOI technology showing the grounds on which the upcoming generations of Si microelectronics will be built. The merits of the leading SOI materials, based on bonding, implantation, or epitaxial growth, will be discussed.

The future trends will be examined in more detail. One way is offered by the continuous shrinking of conventional MOSFETs, which implies a direct scaling of the Si and SiO₂ layers in SOI materials. Although fully-depleted transistors have more potential than partially-depleted SOI MOSFETs, this road will inevitably stop at about 20–30 nm gate length. The second way, far less certain, is to modify the classic architecture of the MOS transistor. Ground-plane and double-gate MOSFETs are straightforward examples which currently attract attention. Different double-gate technologies will be examined together with the physical mechanisms that come into play.

However, other innovative devices can be imagined. Since we will have to live with tunnelling and quantum confinement, the best strategy would be to take advantage of them for constructing totally different types of transistors. We will discuss the 4-gate transistor, the ultimately thin and short MOSFETs (down to a few nanometers), as well as several tunnel-based devices. Preliminary experimental and simulation results will be presented.

Of course, these advanced devices will presumably require a new class of SOI-like materials. For example, in an XOI structure, the silicon film can be replaced by other semiconductors: SiGe, III–V or II–VI compounds, etc. Alternatively, in SOY materials the buried oxide can be traded for other types of insulators: high-K, low-K, sapphire, diamond, glass, plastic, or air. Silicon on Nothing (SON) has recently been proposed as a solution for synthesizing *localized* SOI structures within a bulk-Si wafer. 3-D structures are also envisaged for more compact integration and association of high-speed circuits with optical interconnects. These emerging materials are expected to make feasible novel devices with enhanced performance and functionality.

Before achieving such extreme SOI devices, serious challenges subsist in several domains: availability of ultra-thin SOI films, technology modules, physics-based models, customized libraries for circuit design, etc. A substantial amount of technical effort is still needed to definitely place SOI as the unique survivor of the CMOS technology.

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Title:	F. D'Souza
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Meeting Abstracts Volume 96-1

Title: SOI Technology:
The Future Will Not Scale Down

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