Modelling of Crystal Originated Particles and their impact on Gate Oxide Integrity

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INTRODUCTION

The presence of vacancy defects (voids) in CZ grown substrates is known to correlate well with gate oxide failures. From the typical size and density of the defects (150 nm, 10^6 cm^{-3}) it can be shown that these failures are expected to be caused mainly by voids appearing at the wafer surface (Crystal Originated Particles, COP). This agrees with experimental results, which show that gate oxides fail mainly at positions where surface defects were detected before device fabrication. However, oxides thinner than approximately 5 nm systematically exhibit higher yields than thicker oxides. The aim of the current study is to understand this oxide thickness dependence.

APPROACH

The most common explanations for COP-induced oxide failure are oxide thinning (which causes field enhancement) and field distortion (i.e. non-parallel electric field lines due to electrode curvature). A systematic investigation of these failure mechanisms is complicated by the uncontrolled shape and position of the defects. To solve this, artificial defects were fabricated using an anisotropic etchant, resulting in v-grooves and pits with ⟨111⟩ boundary planes (Fig. 1). Oxide growth in these defects was studied for oxide thicknesses from 4 nm to 15 nm. The impact on the gate oxide integrity was investigated by fabrication of Metal-Oxide-Semiconductor (MOS) capacitors. The thermal oxidation of v-grooves was also simulated using a 2D process simulator. The results were used to calculate the electric field distribution in an MOS structure.

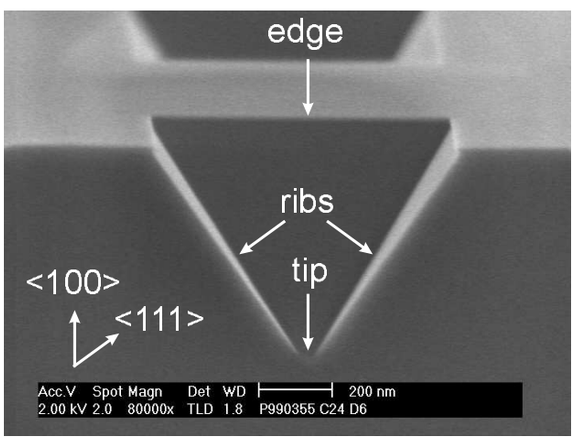

Figure 1: Scanning Electron Microscope photograph of an artificial COP.

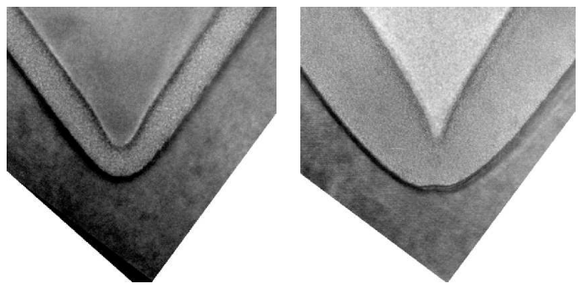

Figure 2: Transmission Electron Microscope photographs of v-groove tips in MOS structures. The oxide thicknesses on the ⟨100⟩ plane are 7.5 nm (left) and 15 nm (right) .

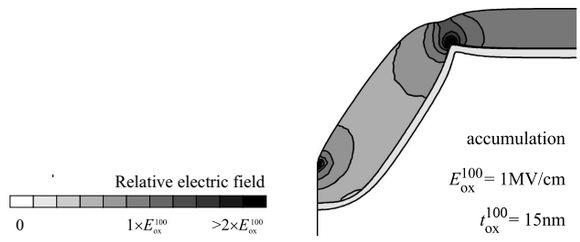

Figure 3: Simulated electric field distribution in a v-groove with a 15 nm gate oxide on the ⟨100⟩ plane. The oxide profile was obtained from process simulations. The field strength is plotted relative to its value on the ⟨100⟩ surface. The tip radius is 10 nm. Because the structure is symmetric, only half of the structure was simulated.

RESULTS

Thermal oxides grown in artificial defects exhibit higher oxidation rates on the ⟨111⟩ planes, and stress limited oxide growth at defect edges and tips (Fig. 2). MOS capacitors containing artificial defects exhibit high gate leakage currents for oxides of 6 nm and thicker. The oxide profiles that were obtained from computer simulations compare well with the experimentally observed profiles. MOS device simulations further indicate a significant increase of the electric field due to the electrode curvature (Fig. 3). Combining the results of the process- and device simulations, the effects of oxide thinning and field distortion can be separated.

CONCLUSIONS

The gate oxide growth in substrate defects is affected by the orientation dependent growth rate and by stress-induced oxide thinning. Both mechanisms enhance the sharpness of convex electrode tips, and consequently lead to field distortion. Field distortion dominates over the field enhancement due to oxide thinning alone, and it explains the experimentally observed polarity dependence of the gate leakage current. For oxide thicknesses below 5 nm, the field distortion is relatively weak, and comparable to the effect of oxide thinning. Moreover, calculations show that electron tunnelling is only moderately affected by field distortion as the tunnelling mechanism changes from Fowler-Nordheim Tunnelling to Direct Tunnelling. These trends provide a consistent explanation for the experimentally observed immunity of thin thermal oxides to the presence of COP.