EFFECTIVE INTRINSIC GETTERING FOR 200MM AND 300MM P/P- WAFERS IN A LOW THERMAL BUDGET 0.13µm ADVANCED CMOS LOGIC PROCESS

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There has been renewed interest recently in the subject of intrinsic gettering (IG) efficiency for low thermal budget processes. High boron concentrations, such as those found in the P+ substrate of a P/P+ epi-wafer are found to enhance the oxygen precipitation rate with the result that the density and size of precipitates produced during the thermal cycle are usually sufficient for effective IG in most device processes. However, for P- and P/P- wafers where the boron concentration is much lower, there is very little opportunity within the device process for oxygen precipitation to occur and so the resulting IG efficiency is very low or non-existent. Another complication is that for 300mm wafers, the manufacturing process requires a double side polishing operation for improved wafer flatness and backside cleanliness. This process flow makes the addition of subsequent back-side extrinsic gettering treatments (soft-backside damage, polysilicon films) for 300mm wafers very costly because the backside must be processed without physically contacting the previously polished front surface. Although the addition of nitrogen or carbon impurities into the starting silicon crystal has been proposed as a method of increasing the amount of oxygen precipitation and IG efficiency, these methods impose additional constraints upon the crystal growth process (1,2).

A very effective alternative method is to use MDZ® (Magic Denuded Zone) technology (3,4). Unlike nitrogen and carbon doping, MDZ® is applied at the wafer level and has been demonstrated to produce consistent bulk micro-defect (BMD) densities and precipitate-free zone (PFZ) depths which are largely independent of initial (Oi), position in crystal and of the device process. The results in this paper will demonstrate that MDZ® is equally effective in 200mm and 300mm diameter wafers.

Experimental

200mm P/P- wafers with and without MDZ® were processed together with 300mm wafers with MDZ® through an advanced 0.13µm CMOS Logic Process. Wafers were withdrawn at the mid-process step and at the end of the process for measurements of delta Oi (initial (Oi) – final (Oi)), bulk micro-defect densities (BMD) and intrinsic gettering efficiency, which was carried out using a nickel haze gettering test.

Results

BMD measurements were obtained for the 200mm P/P- wafers with/without MDZ® and quarter wafers cleaved from 300mm P/P- wafers with MDZ®. No BMDs could be detected after the process itself and so wafers were given an additional 16 hour 1000°C anneal to grow any small precipitates to a detectable size. BMD densities were very low or close to the detection limit for the control wafers at the mid-point and end of process steps. In contrast, radially uniform BMD densities of about $3\text{-}4\times10^{9}$ cm^{-3} were observed for both the 200mm and 300mm wafers with MDZ®.

A nickel haze gettering test (using drops of solutions with nickel concentrations of 10^{11}, 10^{12}, 10^{13} and 10^{14} cm^{-2} on the wafer backsides) at the mid and end of process steps was used to measure gettering efficiency. Haze spots were clearly detectable on the P/P- control at both process stages indicating the lack of intrinsic gettering. In contrast, no haze spots were detectable on either the 200mm or 300mm wafers with MDZ®, demonstrating that the wafers have excellent gettering efficiency. This result is consistent with the observed BMD densities.

Conclusions

1) Very low BMD densities with associated poor intrinsic gettering efficiencies can be expected when standard P/P- wafers (200mm or 300mm) are processed through an advanced 0.13µm CMOS Logic Process.

2) In contrast, radially uniform BMD densities ($3\text{-}4\times10^{9}$ cm^{-3}) were observed for both the 200mm and 300mm P/P- wafers with MDZ®, which resulted in excellent intrinsic gettering efficiencies at the mid-point and end of process steps.

References

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