Impact of State-of-the-art Cz Substrates on the Current-Voltage Characteristics of Shallow p-n Junctions

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1. Introduction. The choice of the starting material certainly impacts on the leakage current (I_R) as already discussed during the previous Conference [1]. Recently, evidence became available that Crystal Originated Particles (COPs) can increase I_R of p-n junction diodes [2], while they also induce isolation failure [3-4]. However, similar as for the gate dielectric, the junction dimensions are being scaled as well, so that one can anticipate that direct substrate related effects on the I-V characteristics of diodes become marginal. In addition, scaling brings along an increase of the peak well doping density in the range 3 to $5x10^{17}$ cm^{-3}, so that the depletion depth for the expected supply voltages is completely contained in this implanted region. The obvious question rises whether one still expects an effect of the starting material quality on the electrical junction characteristics? It is the aim of this work to try to tackle this problem, using shallow junctions in a retrograde p-well, which are compatible with a 0.18 µm CMOS technology.

2. Experimental. The diodes have been fabricated in a variety of 200 mm Czochralski (Cz) p-type wafers, the main features of which are described in Table I. Polysilicon Encapsulated Local Oxidation of Silicon (PELOX) was used for isolation. A retrograde p-well was obtained by a deep ($1.2x10^{13}$ cm^{-2} at 180 keV) and a shallow ($1x10^{13}$ cm^{-2} at 35 keV) boron ion implantation, followed by dopant activation anneal at 850ºC. The n^+-region was made by an arsenic ion implantation ($4x10^{15}$ cm^{-2} at 70 keV), followed by an RTP anneal at 1070ºC. Junctions with different geometry have been studied. A total of four wafers per group were analyzed, containing 43 test chips each.

Table I. Description of the wafer types. The interstitial oxygen (O_i) is calculated according to new ASTM standard.

Material	Substrate ρ [Ohm-cm]	Center O_i [10^{17} at/cm^3] Average	Comment
M1	10 – 18	6.46	high COP
M2	10 – 18	5.91	high COP
M3	7 – 13	6.94	low COP

3. Results and discussion. The current of different geometry diodes is linearly scaling with the area (A), perimeter (P) and number of corners (N_C). Reducing the O_i concentration can increase the yield of the area diode with about 5 %. The effect on the perimeter and corner diode is negligible. On the other hand, it will be shown that reducing the COP density can increase the yield of the area, perimeter and corner diode by 3, 9 and 5 %, respectively. This leads to the conclusion that the yield can be slightly improved in all geometry diodes by reducing the COP density. The impact of O_i on the yield is even more subtle, although some improvement of the area and peripheral component is found for the lower oxygen concentration studied here. As scaling puts more emphasis on the perimeter leakage this could nevertheless be a meaningful result. It is also shown that in low COP material (M3), a 5-10 % lower I_R was found for diodes where I_R is dominated by the peripheral and/or the corner component. The area leaky diodes correspond overall to a hard breakdown I-V characteristic, as defined in Ref. 2 for example. The ones of peripheral and corner, on the other hand, correspond to a so-called soft breakdown curve.

The I_R at –2V of different-geometry diodes corresponding with a cumulative probability of 70 % indicates that the overall yield of all devices studied is very similar for all wafers. It points to the fact that the impact of the substrate on the electrical diode characteristics is rather small and other, processing-related factors are in control, which shows the absence of a clear substrate effect on the characteristics of the average or nominal good diodes. This is supported by a study of the generation and recombination lifetimes in the bulk of the wafers, which is extracted from the diode characteristics. The substrate impact is thus mainly on the yield loss and not so much on the average behaviour.

4. Conclusion. It is concluded here that the average lifetime and current characteristics of deep submicron diodes, fabricated in state-of-the-art substrates with different COP and O_i densities are dominated by the processing-induced defects. The substrate defects have some impact on the diode yield (5-10 %), whereby a lower COP density improves the yield of all diode geometries. On the other hand, reducing the concentration of interstitial oxygen has some impact on the large-area diodes, not so much on the large-perimeter and corner-rich junctions.

5. References

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