

# Integration issues of polysilicon with high k dielectrics deposited by Atomic Layer Chemical Vapor Deposition

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The compatibility and integration of high k dielectrics with polysilicon in conventional CMOS processing, with appropriate thermal budgets is one of the critical issues to implement high k materials into sub 0.1 um front end VLSI device fabrications. The challenges arise from various interfacial reactions between polysilicon and as deposited high k materials during poly deposition at elevated temperature (>500 °C). In addition, interfacial reactions can be further enhanced by subsequent source/drain anneal up to ~1000 °C in CMOS processing. In this work, a systematic approach was adopted to study the various critical issues of poly integration with high k materials deposited by Atomic Layer Chemical Vapor Deposition (ALCVD). The effects of poly deposition conditions, starting growth surface for high k, high k materials and post high k deposition anneal were investigated and correlation obtained between gate leakage and physical/chemical structure characterization.

Effect of starting interface layer for poly- high k interactions is an important factor as shown in fig. 1, where the starting surface modulate the ALCVD growth of ZrO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> with a mechanism of high porosity in the high k films on H-terminated Si, leading to epitaxial overgrowth of Si, whereas potential densification of ZrO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> was achieved on OH-terminated Si such as RTO (Rapid Thermal Oxide) or wet chemical oxide, with a positive impact on interfacial reactions with polysilicon. The surface morphologies and interfacial reactions of poly on ZrO<sub>2</sub> generally improved with decreasing poly deposition temperature and post high k deposition anneal. Issues of permeability to oxygen transport which lead to interfacial oxide built-up and porosity of high k dielectrics also would be required to be seriously addressed in all cases of poly-high k integrations.

Post high k deposition anneal using various gaseous ambient were studied to examine the effect of modification of high k dielectrics for poly integrations. The interfacial oxide built-up was monitored by XPS, interfacial reaction by TEM / MEIS and poly surface morphologies by top-down SEM and haze measurement. For instance, an NH<sub>3</sub> anneal at 700 C was found to give an improved poly morphologies, much reduced poly reactions and no interfacial oxide built up as compared to unannealed high k gate stacks. (cf. Fig. 2)

Electrical measurement of leakage current of poly high k capacitors confirmed these physical characterizations and effects of starting surfaces and post high k deposition anneal. High leakage was observed on ZrO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub>/H-Si stacks as compared with post annealed stacks with OH-terminated Si with a leakage current reduction by >two orders of magnitude. Mixture of Al<sub>2</sub>O<sub>3</sub> and ZrO<sub>2</sub>, on the other hand, is shown to exhibit >fourth orders of magnitude lower leakage current and scalable to ~1.2 nm EOT (fig. 3a-b). Thermal stability of such Zr aluminates is marginal with a 1000 C RTP anneal, other options such as varying Al content, HfO<sub>2</sub>/aluminates and spike anneal methods are currently being investigated.

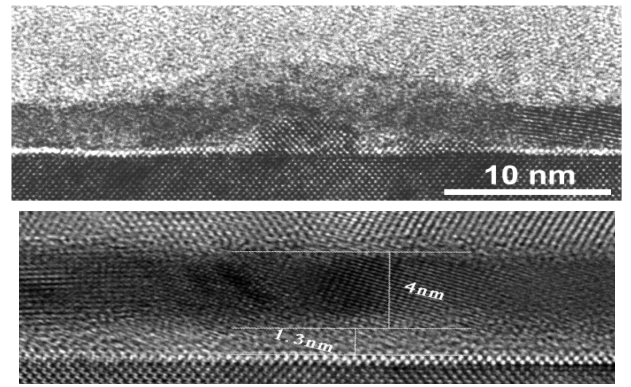


Fig. 1, TEM of n-poly/ZrO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> on H-terminated Si (top) and OH-terminated Si (bottom)

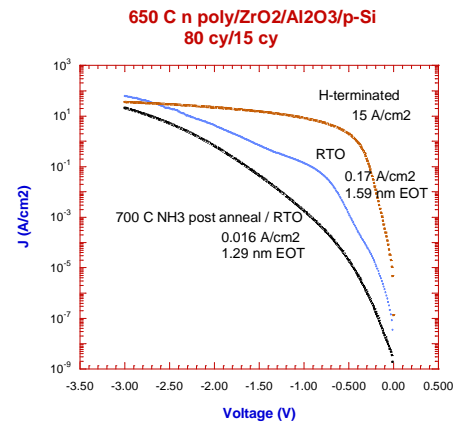


Fig. 2, Leakage through H and OH-terminated interface with deposition annealed ZrO<sub>2</sub>/Al<sub>2</sub>O<sub>3</sub> with Poly-Si/TiN Gate, current density at -1+Vfb.

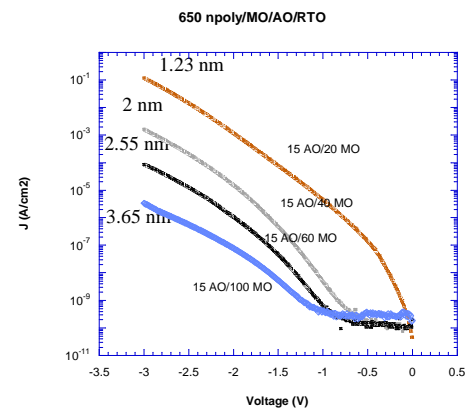


Fig. 3a Leakage and device scaling for mixed oxide with Poly-Si/TiN Gate, current density measured at -1+Vfb.

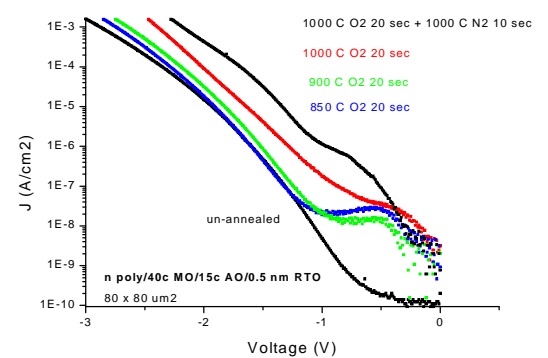


Fig. 3b Leakage comparison for mixed oxide with Poly-Si/TiN Gate as a function of thermal anneal, current density measured at -1+Vfb.