A NEW JUNCTION TECHNOLOGY BASED ON SELECTIVE CVD OF SIGE ALLOYS FOR CMOS TECHNOLOGY NODES BEYOND 30 NM

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Future CMOS technology nodes bring new challenges to formation of source/drain junctions and their contacts. Recently, we have proposed a new technology, which has the potential to address the new challenges[1]. The technology is based upon selective chemical vapor deposition of in-situ doped SiGe in source/drain regions etched to the desired junction depth X_j and it heavily relies on the unique properties of Ge and SiGe. These include improvements in surface chemistry due to the presence of adsorbed Ge atoms, smaller SiGe bandgap, lattice strain and high carrier mobility. Germanosilicides of Ni and Pt are used to form self-aligned, low resistivity contacts to the junctions.

In ITRS, specifications of junctions and their contacts are based on limiting the total parasitic junction resistance to less than ten percent of the channel 'on' resistance. The parasitic resistance is a result of several components, which include: sheet, accumulation, spreading and contact resistance. However, for gate lengths below 65 nm, the contact resistance between the silicide and the junction is the dominant component. For device at the end-of-the-roadmap, contact resistivities as low as 10^{-8} ohm-cm^2 are needed. With a bandgap of 1.12 eV and a boron solubility limit of $2x10^{20}$ cm^{-3}, this is beyond the reach of Si.

The very first advantage of SiGe over Si is its smaller bandgap. Assuming the contact metal has its Fermi level positioned near the SiGe midgap, the contact barrier height is equal to half the semiconductor bandgap. Since contact resistivity is an exponential function of barrier height, a large improvement in contact resistivity can be achieved by a small reduction in barrier height. Figure 1 demonstrates the low contact resistivities obtained using self-aligned contacts of Ni and Pt on boron doped SiGe.

Since dopant atoms are incorporated at substitutional sites during growth, they become electrically active without any subsequent, high temperature annealing. The SiGe layers are deposited at temperatures ranging from 500°C to 800°C. In this temperature range dopant diffusion in Si is negligible - a key requirement for abrupt junctions. The boron profiles shown in Figure 2 indicate an abruptness of ~ 2 nm/decade. The profiles were obtained using secondary ion mass spectroscopy without accounting for the SIMS cascading effect.

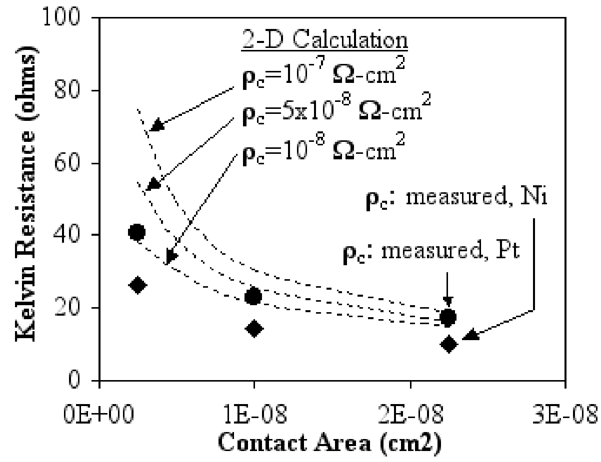

Figure 1 Contact resistivity obtained using self-aligned contacts of Ni and Pt on boron doped SiGe.

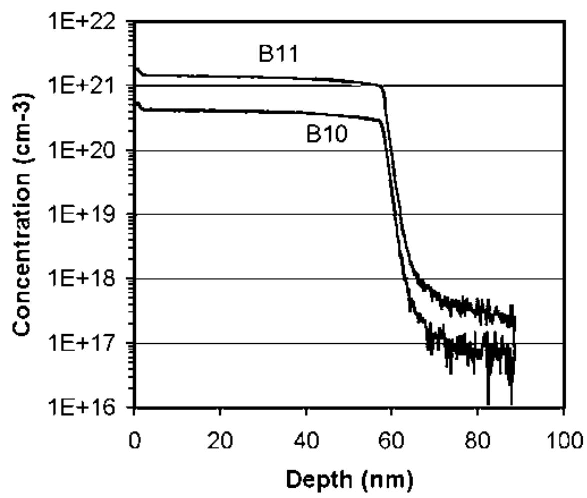

Figure 2 Boron profiles obtained using SIMS.

Another important advantage of SiGe over Si is its ability to provide films with lower resistivities. Junctions formed using the technology comfortably meet the sheet resistance requirements of all technology nodes in ITRS 2001.

In summary, the new junction technology appears highly promising for meeting the demands of the technology nodes beyond 30 nm.

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[1] S. Gannavaram, N. Pesovic and M.C. Öztürk, Low Temperature (≤ 800°C) Recessed Junction Selective Silicon-Germanium Source/Drain Technology for sub-70 nm CMOS", IEDM 2000 Technical Digest