DAMASCENE METAL GATE for 70nm CMOS PROCESS

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Introduction:

The scaling of MOS transistor imposes the reduction of gate length and oxide thickness to continue to improve or at least keep constant devices characteristics. Boron Silicon gate doping, and depletion gate effect have detrimental impact on threshold voltage control and gate oxide capacitance scaling. To overcome this drawback, new material should be used to replace semiconductor gate by metal. Unfortunately metal gate materials are very difficult to integrate in a front-end process mainly due to etching process, stripping, cleaning compatibility, thermal budget to achieve drain and source activation and stability during oxidation step. Based on Back End process a damascene metal gate structure has been proposed [1-2-3], Chemical Vapor Deposition process is chosen to fill the cavity with good step coverage. In this paper we propose a CVD Titanium Nitride followed by a Tungsten (W) CVD shunt for a realistic damascene metal gate CMOS integration.

Process integration

After isolation, well implantations and oxide growth, dummy polysilicon gate is patterned using composite e-Beam and Deep UV lithography. Source and drain extensions are implanted with halos, double nitride spacers and HDD are used to allow good compromise between Short Channel Effect, serial resistance and HDD junction depth for metallization. A dielectric stack is then deposited, first a 7nm pad-oxide followed by 80nm SiN1 borderless layer, then gap fill oxide and 160nm SiN 2 are deposited. A reverse gate mask is used to remove SiN2 on gate larger than 0.5µm. Oxide Chemical Mechanical Polishing is done using SiN1 as landing pad on top of gates, and SiN2 to protect large space without gate from dishing effect. Top of Si gates is cleared with SiN etch back and pad oxide is wet etch before dummy Si gate removal.

Cavity resulting is self aligned on source and drain extensions and it has precisely the same size as the initial Si gate since side walls are bounded by nitride spacers. Gate oxide of 2nm is grown followed by 10nm TiN metal mid gap and 250nm Tungsten shunt material, both deposited by CVD. Metal stack is covered with oxide to prevent dishing during Tungsten CMP. Contact and metallization process steps are done using standard process.

Electrical results :

C(V) plots for both Nmos and Pmos transistors, shows that accumulation and inversion capacitance are very similar demonstrating gate depletion free gate stack. Figure 1 presents a Id (Vg) characteristics for NMOS transistors with retrograde channel doping and Indium halos implanted with a tilt of 42 degrees to enhance SCE induced by low channel concentration. Shortest 40nm gate length presents good channel control with Ioff=30nA/µm at low drain voltage.

Conclusion

70 nm Cmos damascene metal gate using CVD W/TiN process has been successfully integrated. This process will be used to integrate dual metal gate process with high-K materials not compatible with standard Si gates

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References:

[1] A Yagishita et al IEDM 1998, p 785

[2] A Chatterjee et al IEDM 1998, p 777

[3] H Achard et al Proc. ESSDERC 2000, p 408

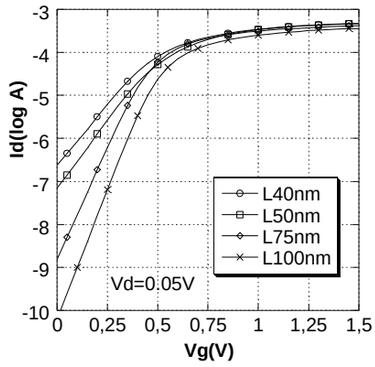

Figure 1 Id (Vg) for Metal transistors with W=10µm and Ld 40 to 100 nm