Defect Management and Yield Enhancement for the Semiconductor Industry

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Defects, particles, and microcontamination – the bane of the semiconductor process engineer! With the urgency to bring new and advanced products to the consumer, there is renewed interest in processing wafers right the first time with high yield. With the advance of 300mm wafer processing and the expense of larger wafers and new more expensive tools, the push for defect-free manufacturing is even more important. There are a battery of *in situ* detection mechanisms in process tools, defect inspection tools, defect review tools, automatic defect classification, and defect management data systems to aid process engineers in their quest for high yielding wafers. Finding the root cause for defects and eliminating them quickly is paramount to keep our industry thriving.

The International Technology Roadmap for Semiconductors (ITRS) has charted very aggressive particle/defect size reductions through the year 2007. For the 100nm technology node expected to be in production in 2003, 66nm for R&D and 88nm for volume production are defect size detection resolutions necessary (1). These numbers require lots of work on the part of the suppliers to build such sensitive tools, and wafer manufacturers to use them to the greatest sensitivity in current defect management practices.

Typical defect management and yield enhancement strategies are multifold. Incoming silicon wafers, as well as thin film monitor wafers, can be scanned with a bright light or laser tool to detect particles and processing defects. This technique requires no extra processing time, and defects as small as 0.12um can be detected. Wafer processing can be monitored directly by means of inexpensive *in situ* particle monitors, inserted in the processing tool itself. The difficulty in the past has been a means to trigger an “alarm” at the occurrence of a particle event, so the problem can be solved immediately before more good wafers are processed through a dirty tool. This technique likewise requires no extra processing time.

There are several different types of tools that are used to inspect wafers after particular processing steps, generally steps that are critical processing steps (for instance, gate etch) or steps where wafers can be reworked if a problem is detected (resist/lithography). Depending on the tool technology and area of the wafer being inspected, this step can take from a minute a wafer to several hours. In general, a sample of a lot is inspected, typically two to three wafers out of a twenty-five wafer lot. Both logic and memory wafers can be inspected with these tools, and sensitivity is around 0.09-0.1um. This procedure, however, does tie up the entire lot until the sample wafers are completed. These wafers usually are then reviewed, either optically or by scanning electron microscope (SEM), and pareto charts kept to monitor wafer processing. Automatic defect classification (ADC) can be utilized to speed up the review process (2). ADC can reside either on the inspection tool or the review tool.

Yet another, but very time consuming technique, is electron beam inspection. This tool provides the best sensitivity (0.8um), but can take up to thirty-six hours for one wafer! This technique is critical for finding electrical defects that would cause a chip to fail either at electrical test or in the field. However, these tools are extremely expensive, take up considerable clean room space, and require a dedicated fab user and field service engineer from the supplier. Therefore, not all semiconductor fabs employ a tool of this type.

Probably the biggest step in this process is organizing all the data into something meaningful for the process engineer. A defect management system (DMS) is crucial to actually determining the root cause of a defect problem. The DMS stores all defect counts, x-y coordinates, defect images, and defect classifications – both by individual wafers and lot. Defect images are linked to specific defects, and lot trend data is available. The inspection/detection tools and DMS allow for integrated yield management for rapid yield learning (3). Utilizing this methodology has historically provided 25-30% per year productivity increase. We will need to work closely with tool suppliers and consortia such as International SEMATECH, SELETE, and IMEC to keep this momentum as we move to 300mm wafer processing.

References

1. The International Technology Roadmap for Semiconductors, Table 78, 2001.
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3. F. Lakhani, Future Fab International, Issue 10, 251, 2001.