50 nm Vertical Replacement-Gate (VRG) nMOSFETs with ALD HfO_2 Gate Dielectrics

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We have integrated HfO_2 gate dielectrics grown by atomic layer deposition (ALD) with poly-Si gate electrodes in the vertical replacement-gate (VRG) MOSFET. These transistors have HfO_2 target equivalent oxide thicknesses (tEOTs) down to 13 Å. The poly-crystalline HfO_2 films in these VRG nMOSFETs exhibit extremely low gate leakage (GL) current densities of $J_G \sim 10^{-7}$ A/cm^2 at V_G–V_T = 0.6 V for 15 Å tEOT devices, more than 10^5 times smaller than found for SiO_2. HfO_2 devices with 50 nm gate length L_G exhibit drive currents (normalized by the coded width W_C [1]) of 490 µA/µm for 1 V operation with good short-channel performance. These results demonstrate that ALD is compatible with the demanding VRG geometry, thereby illustrating that it should be well-suited to essentially any novel device structure built with Si-compatible materials.

The devices were fabricated using the improved core VRG process [2]. All high-T processes (e.g., > 1000ºC source/drain formation) were completed *before* gate dielectric deposition. A 7 Å oxynitride underlayer (UL) was grown on the Si channel, followed by HfO_2 deposition with ALD. A phosphorous-doped a-Si gate was deposited and activated with an 800ºC rapid thermal anneal. The TEM images of Fig. 1 show a completed 50 nm VRG MOSFET with 15 Å tEOT HfO_2. These images demonstrate that the ALD process provides outstanding conformality and is compatible with the VRG structure. Note that the reported tEOT values are determined using physical thicknesses with an assumed permittivity of k = 22 for HfO_2, and *include the intentional 7 Å UL.*

The overall trend of GL vs. tEOT for HfO_2 is illustrated in Fig. 2. The 15 Å tEOT HfO_2 devices show $J_G \sim 10^{-7}$ A/cm^2 for 1 V operation. This is more than 10^5 times smaller than found for SiO_2 [3]. Extrapolation of the measured trend suggests that HfO_2 should be scalable to ≤ 10 Å tEOT. These low leakage currents are especially encouraging since they have been measured in a VRG structure, where the gate dielectric-channel interface has not been optimized to the same extent as in planar devices. Moreover, the extremely low gate leakage of the poly-crystalline HfO_2 indicates that *amorphous* gate dielectrics *may not* be necessary to meet GL requirements. The performance of a 50 nm VRG nMOSFET with 15 Å tEOT HfO_2 is shown in Fig. 3. This device has a respectable s = 97 mV/dec, and it drives I_D/W_C = 490 µA/µm at V_{GS}-V_T = 0.6 V and V_{DS} = 1 V. Significant improvements are expected from further optimization of the VRG process.

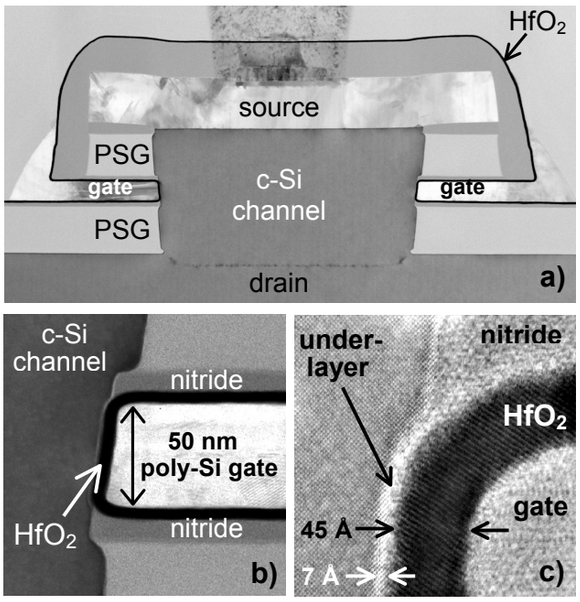

Fig. 1. a) Bright-field TEM image of a completed 50 nm VRG nMOSFET showing the highly conformal HfO_2 layer. **b)** Higher magnification image of the active area. The very dark color of the HfO_2 is due to strong scattering by the heavy element Hf. **c)** Atomic resolution image of the top corner of the gate, indicating the crystalline HfO_2 and underlayer thicknesses. The lattice planes of a HfO_2 grain which turns this corner are visible.

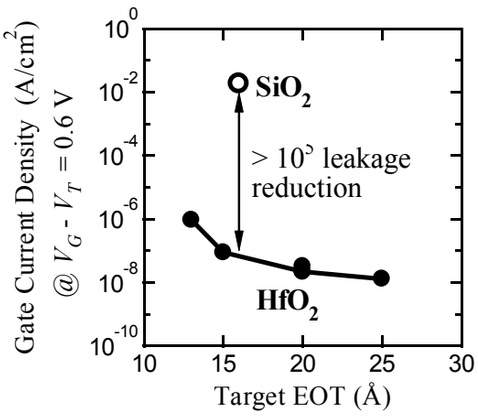

Fig. 2. Gate leakage (GL) for HfO_2 and SiO_2 measured in inversion at 0.6 V above threshold (i.e. what an nMOSFET sees for ≈ 1 V operation). The GL for HfO_2 is more than five orders of magnitude lower than that of SiO_2. The HfO_2 trend suggests that in the VRG structure, HfO_2 can scale to tEOT ≤ 10 Å while maintaining a gate current density below 1 A/cm^2.

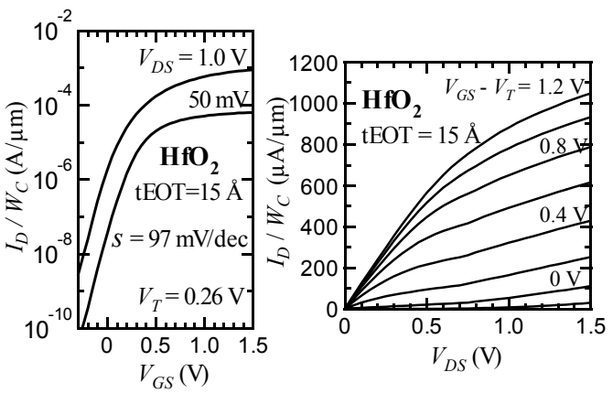

Fig. 3. Subthreshold and I_D-V_{DS} curves for a 50 nm VRG nMOSFET with HfO_2 (target EOT = 15 Å). Devices from this wafer are shown in the TEM images of Fig. 1.

References

[1] J.M. Hergenrother *et al.*, *IEDM Tech. Dig.*, p. 75 (1999).
[2] Sang-Hyun Oh *et al.*, *IEDM Tech. Dig.*, p. 65 (2000).
[3] J.M. Hergenrother *et al.*, *IEDM Tech. Dig.*, p. 51 (2001).