Lateral Oxidation Kinetics of $Al_xGa_{1-x}As$ Layer by Capacitance technique

N.C. Das, B. Gollschneider, P. Newman and W. Chang
Army Research Laboratory, AMSRL-SE-EM, 2800 Powder Mill Rd., Adelphi, MD 20783

Capacitance voltage (C-V) technique is used to determine the kinetics of lateral oxidation of $Al_xGa_{1-x}As$ layer in circular mesa structure. The oxide layer width determined by C-V technique agrees with optical measurements. Additionally C-V technique has advantage of determining different types of defects in the oxide which is important for reliability of vertical cavity surface emitting laser (VCSEL) devices.

Recently wet oxidation of AlAs (or AlGaAs with high Al content) has generated intense interest in term of its physical properties and device application due to optical mode and current confinement of laser structure. This stable native oxide can be formed by various techniques: such as dry or wet oxidation, anodic oxidation and chemical oxidation. For current confinement in VCSEL structure, oxidation is done for few micrometers from the edge of the mesa structure. There exist considerable controversies whether oxidation follows linear or parabolic growth rate. Kim et al reported linear growth rate for different Al mole fraction and also they showed oxidation rate strongly depend on AlAs thickness. On the other hand Ochiai et al reported a parabolic growth rate at longer oxidation time.

The lateral oxidation width in GaAlAs mesa structure is measured either by optical or scanning electron microscopic technique. However in actual VCSEL structure optical method can not be used as the oxide layer is few micron below the top surface layer. Also SEM technique is time consuming and also sample is prepared by cleaving which is a destructive technique. We report here the capacitance-voltage technique to determine the lateral oxidation width as well as various traps in the oxide. This technique is compatible with VCSEL fabrication process and hence can be implemented through the test structure in the wafer. It is found that negative charges are produced during wet oxidation process which agrees with previously reported results.

The epitaxial structures used in this study were grown by molecular beam epitaxy technique on N-plus GaAs substrate. Different mesa structures were lithographically defined using a test mask and wet chemical etching. The mesa structure ranges from 25 to 60 micron diameters. Wet oxidation was carried out in the temperature range of 400-435 °C with nitrogen carrier gas bubble through H_2O at 85 °C. It is well known that oxidation moves inwards starting from the edge of the wafer with increasing time. After oxidation, the AlGaAs oxide layer is converted to native oxide and hence its refractive index is changed. Hence the color of the oxidized layer is different from the unoxidized layer. After oxidation Ti/Au (300/2500 Å) was deposited as p-type contact metal on top side and Ge/Au metal film was deposited as n-type metal on backside of the wafer. The wafer was annealed at 400 °C for 60 sec. in forming gas by rapid thermal annealing technique.

The high frequency (1MHz) capacitance-voltage curve was taken by using HP 4280 A meter. After mesa etching both top and bottom contact metal was deposited. The C-V curves shown here are from p-n junction mesa structure without any thermal oxidation layer. The capacitance decreases with decrease of area linearly and shows depletion layer capacitance at gate bias less than 0 volt. With increase of positive voltage greater than 0 Volt, capacitance increases with inversion layer capacitance and for voltage greater than 2.0 Volt, capacitance decreases as the conductance increase due to the forward bias condition of p-n junction. The onset of inversion occurs at about 1.0 V for all these curves. The depletion layer width stays same for large reverse bias voltages of 0 to –5.0 V as it is evident from constant capacitance in the voltage range. Unlike unoxidized mesa structure, the C-V curves for oxidized mesa shifts to higher positive values compared to unoxidized mesa C-V curve, indicating negative charges present in the oxide. From the observed shift of 0.3 V in case of C-V curves for 10 min. oxidation at 400 °C, the calculated oxide trap density is $2X10^{11}/cm^2$. For higher oxidation time (80 min.) capacitance curve shifts so much positive that we saw very little increase in capacitance at positive voltage of 2.0 V. However, the depletion layer capacitance for negative biases (for voltages below 0 V) decreases with increase of oxidation time. This is due to the change in capacitance due to oxide layer formed in the mesa structure. This change in depletion layer capacitance is used to measure the width of the oxide layer at different oxidation time.

At present, we do not know what is the origin of this negative charge in the oxide, which increases with higher oxidation time and temperature. For reduced oxide charge of same oxide width, it is advisable to use lower oxidation temperature

In summary a new approach to measure the oxidation kinetics is proposed for GaAs mesa structure. This method can be used to measure the oxidation width in VCSEL mesa structure as well as the oxide trap density. This is essential in determining VCSEL reliability. Longer oxidation time not only result in higher oxidation width but also higher oxide trap density. We observed a linear oxidation growth rate for shorted oxidation time and a parabolic growth rate at longer time. Since annealing in nitrogen environment reduces both trapped charge and interface density, annealing may be used to achieve low voltage VCSEL operation.

Acknowledgements: We thank P. Shen and G. Simonis for many useful discussions.