Challenges and Opportunities in high-k Gate Dielectric Technology

Masaaki Niwa,[1] Yoshinao Harada,[1]
Kazuhiko Yamamoto,[1] Shigenori Hayashi,[1]
Riichiro Mitsuhashi,[1] Koji Eriguchi,[1]
Masafumi Kubota,[1] Yasuaki Hoshino,[2]
Yoshiaki Kido[2] and Dim-Lee Kwong[3]

[1]Semiconductor Company, Matsushita Electric Industrial Co.,Ltd.
19 Nishikujo-Kasugacho
Minami-ku
Kyoto 601-8413
Japan

[2]Department of Physics, Ritsumeikan University
Nojihigashi
Kusatu
Shiga 525-0058
Japan

[3]Microelectronics Research Center, The University of Texas at Austin
10100 Burnet Road
Austin, TX 78758
USA

Challenges and Opportunities in high-k Gate Dielectric Technology

Masaaki Niwa1, Yoshinao Harada1, Kazuhiko Yamamoto1, Shigenori Hayashi1, Riichiro Mitsuhashi1, Koji Eriguchi1, Masafumi Kubota1, Yasushi Hoshino2, Yoshiaki Kido2 and Dim-Lee Kwong3

E-mail: niwa@krl.mec.mei.co.jp

1ULSI Process Technology Development Center, Matsushita Electric Industrial Co., Ltd. Minami-ku, Kyoto 601-8413, JAPAN

2Department of Physics Ritsumeikan University Kusatsu, Shiga 525-8577, JAPAN

3Department of Electrical and Computer Engineering The University of Texas at Austin Austin, TX 78712, USA

CMOS technology is projected to continue aggressive scaling down to less than 45nm gate length. On the other hand, compared to the present CMOS technology, improvement of the device performance is increasingly difficult. Major reason for this is due to small margin between Ion and Ioff. In order to achieve an ultra-thin equivalent oxide thickness (EOT) with an acceptable low electrical leakage, gate dielectric has emerged as one of the most difficult challenges for future device scaling. In addition, an important issue with a material other than SiO2 is that a very thin gSilicon oxideh layer may still be required at a channel interface to preserve channel mobility as well as interface-state characteristics. However, this would lead to severe degradation of any benefits of introducing of high-k gate dielectric thereby increasing of the EOT. A single molecular layer of Si-O bonding to bridge between the silicon substrate and a high-k dielectric material would present a physical limit to scaling of EOT to no less than approx. 0.3nm. In addition, it is also anticipated that an appropriate material may be required for the upper interface between the high-k dielectric and the gate electrode. Improvement of thickness control as well as uniformity for the high-k dielectrics are also essential to achieve Vt control for 300mm wafers. And, as for reliability for the high-k gate dielectrics, it seems too early to discuss in detail since gate electrode material is not yet decided as well as the high-k material itself.

From these respects, although high-k material will brings us a best solution for future gate dielectrics, still many items to be overcome remained.

In this paper, we pick some of the critical issues up and discuss on our recent results on high-k film. In addition, we look into some aspect on high-k research in Japan that are addressing these issues. Also, we discuss about an opportunity of high-k introduction based on technical trend appeared in ITRS2001[1].

The issues we address are 1) Timing of introduction of high-k gate dielectric

2) Influence of the stress at oxide/Si interface on reliability

3) Control of the interfacial layer thickness

4) Study on breakdown phenomena

5) Other important issues on high-k gate stack process

6) Aspects of research activities on high-k in Japan.

REFERENCE 1. Int. Tech. Roadmap for Semiconductors, 2001 Edition.