**Stability of Advanced Gate Stack Devices**

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Advances in silicon ULSI technology have been on aggressive trends in past years. In order to satisfy the gate leakage specifications in the International Technology Roadmap for Semiconductors (ITRS), several alternative gate stack materials have been proposed. Here we report on the stability of alternative gate stacks, primarily $HfO_2$, fabricated using a gate last process. $HfO_2$ was deposited by PVD, and Poly-Si was prepared by 600°C LPCVD followed by ion implantation and dopant activation using 900°C 60sec RTA. The $HfO_2$ had an equivalent oxide thickness (EOT) of 12 nm.

After device fabrication, the stability was evaluated by uniformly injecting current and monitoring device characteristics during stressing. The stressing was accomplished under the polarity used for normal NMOS operation (shorting the source, drain, and substrate and applying a positive gate bias).

Fig. 1 plots the shift in threshold voltage and peak transconductance as a function of injected charge. As the amount of injected charge increased, the threshold voltage increased and the transconductance decreased. The subthreshold threshold slope was not degraded. A power-law dependence was observed between the threshold voltage and the injected charge (J•t),

$$\Delta V_t \alpha (J \bullet t)^n$$

where the power dependence, n was about 0.1 for the fields used here. Extrapolation to 10 years of stressing ($3x10^7$ C/cm$^2$ at the 0.1 A/cm$^2$ ITRS specification for low standby power applications) gave a total shift of about 200 mV, corresponding to about $3.5x10^{12}$ trapped charges/cm$^2$. It should be noted that the neutralization of fixed positive charge, i.e., that having a coulombic capture cross section of about $10^{-13}$ cm$^2$, should have saturated at much lower injected charge levels than those reported here. Thus the shifts seen in Fig. 2 must represent the filling of neutral traps having a very small capture cross section or the generation of new charge centers in the dielectric or at an interface.

Figures 2 and 3 shows mobility curves and the extracted values of the scattering parameters (interface charge and surface roughness) using a MOSFET device parameter analysis program with corrections for quantum mechanical effects [1]. The scattering parameters also appear to obey a power-law dependence on the injected charge. Although the coefficient describing the increase interface scattering charge is about the same as that for the increase in charge influencing the threshold voltage, the number of scattering centers is only about 60% of the total charge observed from threshold voltage shifts. Also, the analysis suggests that the interfacial roughness scattering is reduced by the injection of the charge; but it is not clear if there is any physical mechanism that would result in a smoother interface. Instead the observation raises additional questions about the classical interpretation of mobility data in alternative gate stack devices

Preliminary attempts to evaluate the stability of group III oxides (MBE-deposited $La_2O_3$ and RPECVD-deposited $Y_2O_3$) were less successful. For one thing, breakdown frequently occurred immediately after stressing at 0.8 A/cm$^2$. In addition, these materials exhibited a discrepancy in EOT between that extracted from capacitance-voltage data and that inferred from device mobility data. (By matching experimental device I-V data to a theoretical mobility curve that uses the default scattering parameters, i.e., those for good oxide, one can put an upper bound on EOT). The EOT inferred from I-V data were less than those extracted from C-V.

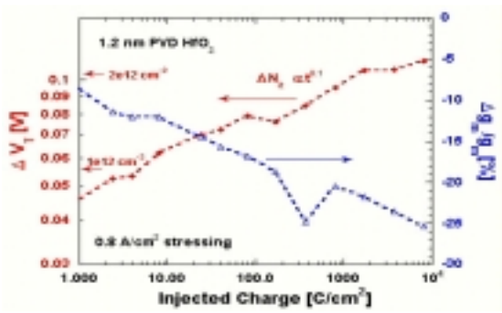


Fig. 1. Threshold voltage and transconductance shifts made with 1.2 nm $HfO_2$ gate dielectric.

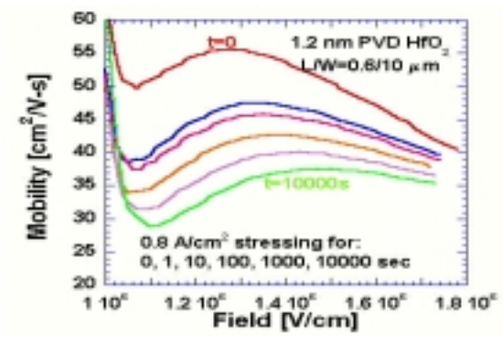


Fig. 2. Mobility shifts for the devices made with 1.2 nm $HfO_2$ gate dielectric.

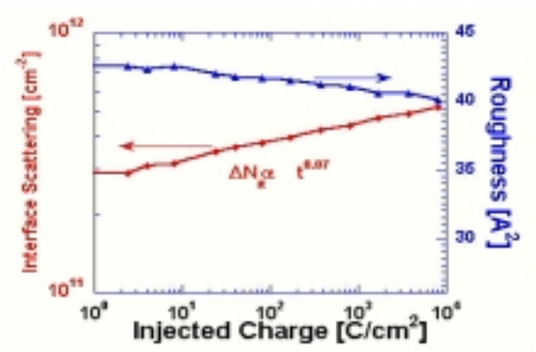


Fig. 3. Effect of stressing on interface scattering and roughness parameters of devices made with 1.2 nm $HfO_2$ gate dielectric.

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Reference

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