Flat-band Voltage Study of High-K Dielectrics Subjected to Spike Thermal Annealing

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High-K dielectrics, based on oxides of Al, Hf, and Zr, were prepared by atomic layer deposition (ALD) on 200-mm Si wafers in an ASM production reactor. Films were deposited directly on clean Si or on underlayers of various thin (0.5 nm) rapid thermal oxides or oxynitrides of Si. The purpose of the underlayer films is to provide a barrier for charge penetration from the crystal Si to the high-K dielectric film. Deposited Al-oxide films varied in thickness from 2 to 6 nm. Post deposition anneals were used to stabilize the ALD oxides. Equivalent oxide thicknesses varied from 1 to 3.5 nm. Pure thermal oxides were included in the study for reference. In situ-doped amorphous-Si 160 nm films were deposited over the oxides to prepare heavily-doped gate electrodes in MOS structures. In a first study both the Si wafer substrate and gate electrode were n-type. Samples were annealed in a Heatpulse RTA system in N2 ambient at 800 C for 30 s, or spike annealed at 950, 1000,and 1050 C (nominally zero time at peak temperature). Heating and cooling rates are approximately 50 C/s. Flat band voltages (VFB) were determined from C-V measurements on dot patterns. The 800 C anneals were used as a baseline, at which the poly-Si electrodes are crystallized and acquire electrical activation while subjecting the high-K dielectrics to a low thermal budget. For P doped poly-Si electrodes and Al-oxide based dielectrics, positive shifts in VFB were observed, relative to a pure SiO2 control, ranging from 0.2 to 0.8V. The shifts are believed to arise from leakage charge trapping in the dielectric. Spike anneals at 1000 C tend to decrease VFB relative to VFB for the 800 C anneal. Changes in VFB up to 0.35 V are observed for ALD films deposited over underlayers, while smaller changes, up to 0.05 V, are observed for ALD film deposited directly on Si. Spike annealing is also observed to reduce oxide leakage.