Effect of Post Metallization Annealing for Alternative Gate Stack Devices

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To meet the gate leakage specifications in the International Technology Roadmap for Semiconductors (ITRS), an intensive search is being conducted for alternative gate stack materials. Most of the studies have focused on basic material properties, but very little effort has been directed towards quantifying and understanding the effect of post metallization annealing (PMA) on the electrical properties of the dielectric. In this work, devices were fabricated with a "gate last" process. The gate dielectrics studied included: HfO_2 deposited by PVD or MOCVD, as well as Y_2O_3 and La_2O_3 deposited by RPECVD and MBE, respectively. Poly-Si gate electrodes were prepared by 600°C LPCVD followed by ion implantation and dopant activation using 900°C 60sec RTA. Device characteristics were measured before and after 20 min 400-450°C forming gas (FG, 10% H_2 in N_2) annealing. To verify the role of hydrogen in PMA, some devices were annealed in nitrogen only. Capacitance versus voltage (CV), gate leakage current, drain current versus gate voltage, and drain current versus drain voltage were measured. MOSFET device parameter analysis programs with corrections for quantum mechanical effects [1, 2] were used to extract key device parameters: equivalent oxide thickness (EOT), metal-to-semiconductor workfunction, substrate doping, channel mobility as a function of electric field, number of interface scattering charges (N_{if}), and the interface roughness scattering parameters (L*H product).

PVD HfO_2 (1.2 nm EOT) with Poly Si gates exhibited only a minor change in CV and gate leakage current after the 400°C FG PMA. Likewise, the device threshold voltage shift was negligible. But as shown in Figs. 1 and 2, there was a dramatic enhancement in the device current and about 46% higher mobility, which was interpreted in terms of reduced charge ($8e10^{10}/cm^2$after PMA versus $1.2e10^{11}/cm^2$before) and roughness scattering ($39Å^2$ after vs. $65Å^2$ before). As a reference point, high quality oxide might typically have $3e10^{10}/cm^2$ interface charges and $25Å^2$ of roughness scattering; thus PMA of this HfO_2 was not sufficient to give as high a mobility as SiO_2. Nevertheless, the forming gas anneal in this case does seem to eliminate interface states between HfO_2 and the substrate, resulting in higher current and mobility.

For the group III materials with poly-Si gates (MBE La_2O_3 and MOCVD Y_2O_3), post metallization annealing also resulted in higher device current. For La_2O_3, PMA shifted both the flatband and the threshold voltages by the same amount (300mV) indicative of a reduction in fixed oxide charge. On the other hand, Y_2O_3 showed a 200mV shift only in the threshold voltage—not in the flatband voltage. The EOT values from CV data resulted in anomalously high values of mobility. Here the mobility parameters, including EOT, were extracted from device I-V data based on the assumptions that: a) EOT was not affected by PMA and b) the post-PMA scattering parameters were the same as good SiO_2 ($3e10/cm^2$). Peak mobility of 63% and 57% higher were observed for La_2O_3 and Y_2O_3, respectively. Dramatic reductions in interface scattering charges were observed: from 19 and 11 $e10/cm^2$ for Y_2O_3 and La_2O_3 respectively, to $3e10/cm^2$. The roughness scattering parameters did not change much. It seems that the FG post metallization annealing reduces interface charge also for group III materials. The gate leakage was not affected by PMA for either material.

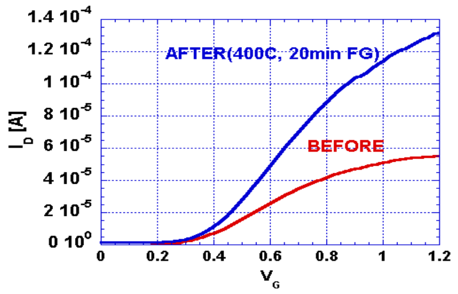

Fig. 1. I_d-V_d characteristic of PVD HfO_2 and Poly-Si devices before and after PMA. (V_{dd} = 50 mV)

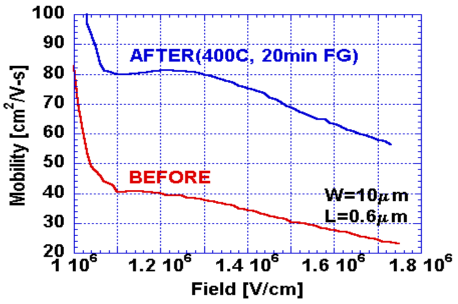

Fig. 2. Mobility of PVD HfO_2 and Poly-Si devices before and after PMA

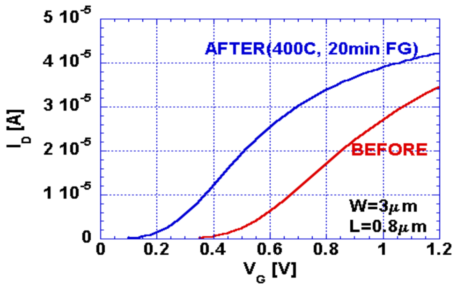

Fig. 3. I_d-V_d characteristic of MOCVD Y_2O_3 and Poly-Si devices before and after PMA (V_{dd} = 50 mV)

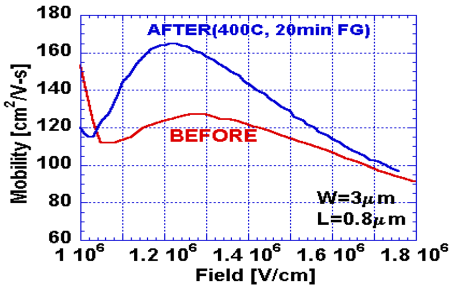

Fig. 4. Mobility of MOCVD Y_2O_3 and Poly-Si devices before and after PMA

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