HIGH-k GATE DIELECTRIC MATERIALS FOR ADVANCED CMOS DEVICES

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As CMOS devices are scaled beyond the 100 nm node alternate gate dielectrics will be required to replace current nitrided SiO_2 gate dielectrics owing to the high gate leakages as a result of tunneling through the thin dielectric [1]. Most of the recent research on high-κ gate dielectrics has concentrated primarily on binary metal oxides such as Al_2O_3, ZrO_2, HfO_2, silicates and their nanolaminates [2]. These materials offer a number of desirable characteristics that make them suitable to investigate as potential replacements for conventional gate dielectrics. However, published data on ZrO_2 [3], HfO_2 [4], and Al_2O_3 [5], shows that dopant penetration in both of these materials is a problem. The binary oxides also tend to have low crystallization temperatures, in most cases less than 1000°C. Crystallization may enhance dopant diffusion and may promote degradation during device operation. It is for this reason that amorphous materials may be preferred as gate dielectrics. Recent data on ZrON [3] indicate that boron penetration may be minimized by the introduction of nitrogen similar to the case of SiON. The objective of this paper is to present initial data on HfSiON a new amorphous gate dielectric that addresses some of the problems encountered by other high-κ gate dielectric materials.

Fig. 1 shows XRD scans of ~100Å thick HfSiON and HfSiO films with the corresponding high-resolution TEM images. The XRD pattern clearly shows the presence of a crystalline peak in the case of HfSiO after annealing at 1000°C while no peaks are observed in the case of HfSiON that was annealed at 1100°C. Fig. 2 shows a ToF-SIMS depth profile of a thick HfSiON film. This indicates that nitrogen can be incorporated uniformly throughout the film. MOS capacitors have been fabricated with this dielectric for both n-channel and p-channel devices using a conventional flow. The leakage current density of HfSiON is much lower than SiO_2 as shown in Fig. 3. Further improvements in EOT scaling and leakage current reduction can be achieved by process optimization. The leakage mechanism of these films is predominantly Frenkel-Poole as is the case for most high-k gate dielectrics [6]. The C-V curves shown in Fig. 4 for both p and n MOSCAPs show low interfacial traps but the flat band voltage of the pMOS devices is shifted. The flat-band voltage shift of the pMOS devices is not clearly understood and as with other high-κ gate dielectrics requires more attention.

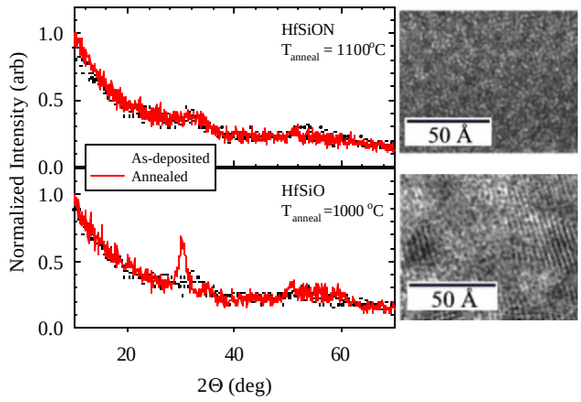

Fig. 1. a) X-ray diffraction patterns of HfSiO and HfSiON before and after annealing with a corresponding TEM image after annealing at 1000°C for HfSiO and 1100°C for HfSiON.

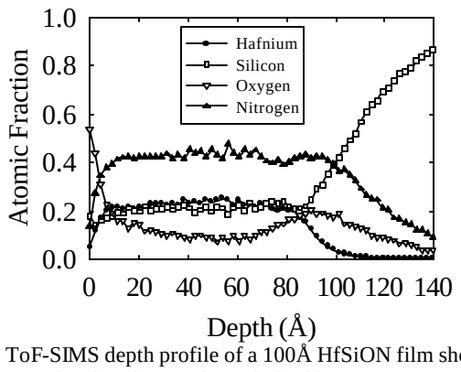

Fig. 2. ToF-SIMS depth profile of a 100Å HfSiON film showing Hf, Si, N, and O distribution through the film.

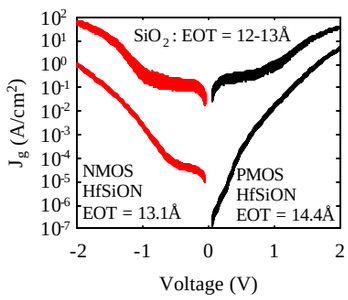

Fig. 3. J_g-V curves of p and nMOSCAPs fabricated with HfSiON gate dielectric in a conventional MOS flow using poly-Si gate electrodes. Each family of curves represents 98 devices.

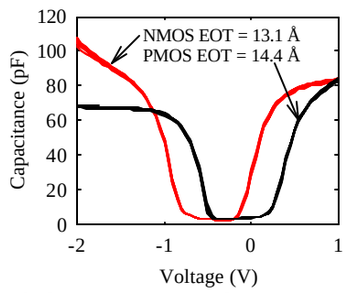

Fig. 4. Dual frequency corrected C-V curves of p and nMOSCAPs fabricated with HfSiON gate dielectric in a conventional MOS flow using poly-Si gate electrodes. Each family of curves represents 18 devices.

References

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