

NMOS Gate Electrode Selection Process for Advanced Silicon Devices

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As gate oxide thickness decreases, the capacitance associated with the depleted layer at the poly-Si/gate dielectric interface becomes significant, making it necessary to consider alternative gate electrodes [1]. Metal gates must have compatible work functions, ϕ_m (~4.1eV for NMOS and ~5.0eV for PMOS), process compatibility and thermal/chemical interface stability with the underlying dielectric. While several PMOS candidates have emerged, metals with NMOS compatible work functions (Zr, Hf, Ti, Ta, etc) typically suffer from thermal instability owing to their high affinity for metal oxide formation [2]. One option to achieve this is to introduce N in metals. It has been shown from Cu barrier layer studies that the presence of N can effectively retard reaction rates, provide better diffusion barrier properties and result in smoother microstructures. The use of N in metal can then be advantageous provided that the workfunction is not increased significantly. In our work, we have demonstrated that the addition to N in Ta films indeed improves their thermal stability with a tradeoff of ~0.2eV larger workfunction. However, at very high temperatures and high N contents, N diffusion to the Si-SiO₂ interface is observed. The TaN_x alloy can be further stabilized by the addition of silicon, which not only improves the diffusion barrier properties but also retards grain growth compared to TaN_x films. An amorphous or nanocrystalline grain structure film can have intrinsically better interface stability since grain boundaries can act as oxygen scavenging sites. In addition, we have found that TaSiN alloys can result in low work function values provided the Ta/Si ratio in the films is <1. The presence of Si prevents N diffusion to the underlying Si-dielectric interface both for thin dielectrics and under high temperature processing. However, the Si content must be carefully optimized since excess Si can result in a) high resistivity and b) the formation of TaSi₂ at the gate dielectric/gate electrode interface resulting in a high work function film (~4.8eV). Since both TaN and TaSiN have already been considered as Cu diffusion barriers in the backend, they are strong candidates for gate electrodes as well. The results of TaN_x and TaSi_xN_y gates on both SiO₂ and high-K dielectrics will be discussed and compared.

An alternate route in obtaining low work function films is by alloying of elemental metals. For example, optimized binary alloys can provide desired work function with good thermal stability. This approach avoids the use of N, which can diffuse under high thermal budgets, or Si, which can lead to the formation of di-silicides with large work functions. The binary metal alloys system should be chosen such that a stable single phase can be obtained in a large window of concentration. Results will be presented on binary alloys of Ta-Ru. It was found at at. Ta% between 40 and 54% produces a single Ru₁Ta₁ phase,

which has a work function of 4.3 eV with excellent thermal stability, making it a viable candidate for NMOS devices. Figure 1 shows the workfunction as extracted from the intercept of V_{FB} vs EOT curves as a function of Ta percent power in Ru-Ta alloys after anneals at 800°C, 900°C and 1000°C. Alloy films with Ta > ~60%, exhibited a work function change (as extracted using V_{FB} vs. EOT) under high temperature anneals. This change was also confirmed by barrier height measurements. This change was attributed to the formation of TaSi₂ at the top interface. No such change was observed for Ta less than 60% and films with at. % Ta < 54% displayed excellent thermal stability. Since films with at. % Ta between 40% and 54% were also found to have low work functions, they are worthwhile candidates for NMOS devices.

1. J. R. Hauser et al, SRC working paper, 1997.
2. V. Misra, G.P. Heuss, H. Zhong, "The use of MOS Capacitors to Detect Interactions of Hf and Zr gate with SiO₂," Appl. Phys. Lett. Vol.78, p. 4166-4168, 2001.

