Cutting-edge temperature measurement and control over a wide range of process temperatures in a 300 mm hot-wall RTP system.

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State-of-the–art temperature measurement and control in rapid thermal processing (RTP) continues to be a necessity for meeting the device performance requirements for larger wafer sizes and smaller device nodes. A new 300 mm dual chamber hot wall RTP tool, called the Summit 300XT, utilizes robust measurement and control of wafer temperature. In this work we demonstrate how this system addresses three main challenges for temperature measurement and control for current and future device nodes: 1) Independence of process results to backside emissivity, 2) Temperature control for spike anneals, and 3) Temperature measurement and control of low temperature processes.

Summit 300 adjusts the wafer temperature by controlling the position of the wafer in a furnace based hot-wall thermal gradient environment as shown in Figure 1. The emissivity compensated pyrometry based temperature measurement system works in conjunction with a feed-forward model based temperature control system to measure and track the desired wafer temperature trajectory. We describe the fundamental advantages of the unique non-reflective, quasi-isothermal environment of the hot-wall RTP system. The non-reflective nature of the system allows the measurement of the free space emissivity. We also describe the principles behind the temperature measurement and control system, and the improvements in optics and signal processing hardware which enable the state-of-the-art performance.

The performance of the system in the three areas described above is demonstrated. This paper describes the demonstration of emissivity independence via growth of thermal SiO_2 on wafers with various film stacks deposited on the backside. Figure 2 illustrates the repeatability of oxide film thickness for wafers with an emissivity range from 0.2 to 0.95. Outstanding high temperature within-wafer uniformity as well as across-cassette repeatability is shown through process data from dwell and spike anneal and thermal oxidation. Figure 3 shows process repeatability in peak temperature for a spike anneal process. Finally, data showing excellent temperature measurement and control for low temperature processes is presented. Data showing excellent within wafer uniformity for low and high temperature processes is also presented.

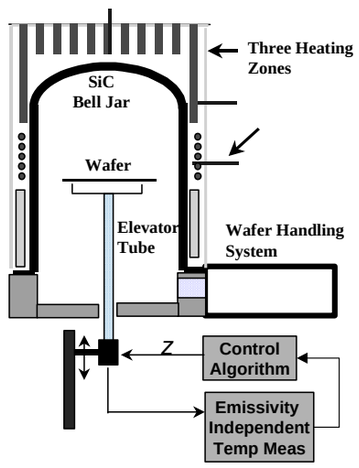

Figure 1

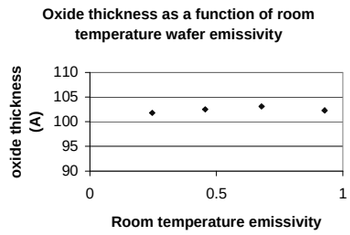

Figure 2

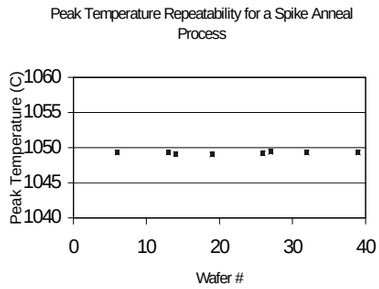

Figure 3