Carbon Nanotube Charge-Storage Memory Devices

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Single-walled carbon nanotubes (SWNTs) – nanometer-diameter wires of pure carbon – are attracting significant interest for their possible use in nanoelectronics applications. SWNTs may be metallic or semiconducting depending sensitively on how the graphene lattice is wrapped to form the nanotube(1). A number of SWNT-based electronic devices have been demonstrated, including single-electron transistors (SETs) (2), field-effect transistors (FETs) (3), and junction devices(4).

The prototypical SWNT FET (tubeFET) consists of a single semiconducting SWNT on an insulating substrate, contacted at each end by metal electrodes. A nearby electrode, either buried under the substrate or to the side of the nanotube channel, acts as a gate. TubeFETs may have high transconductances, and TubeFET logic devices with greater than unity gain have been demonstrated(5).

Here we report on the first attempts to use a tubeFET as a charge-storage memory device. Our devices operate by injecting electrons from the nanotube channel of a tubeFET into charge traps on the surface of the SiO_2 gate dielectric, thus shifting the threshold voltage. This memory can be written and erased many times, and has a hold time of hundreds of seconds at room temperature. We expect that this device can be significantly improved upon by a suitable choice of charge-trapping medium, such as a floating gate or oxide-nitride-oxide structure, and these experiments are underway.

Devices were prepared on degenerately-doped silicon substrates capped by 500-1000nm of thermally grown SiO_2. SWNTs were grown on the substrates using chemical vapor deposition at 900-1000ºC, with methane as the feedstock gas(6). Alignment marks were patterned on the substrate using electron-beam lithography, and SWNTs were located relative to the alignment marks by atomic force microscopy. A second electron-beam lithography step established Cr/Au electrical contacts to individual SWNTs.

Figure 1 shows the conductance of the SWNTs was measured as a function of voltage applied to the silicon substrate (gate). The overall behavior is that of a p-channel depletion-mode transistor, as previously seen in tubeFET devices(3). The conductance is hysteretic in gate voltage; swings of ±10V in gate voltage produce approximately 2V shift in threshold voltage. This hysteresis forms the basis of the memory device.

The memory effect is demonstrated in Figure 2. Here the device is biased at 100mV, and the current and gate voltage are shown as a function of time. The gate voltage is held at +2.5V to read the state of the device, and pulses of +10V or -10V are applied momentarily to write the device to a "1" (high conductance) or "0" (low conductance) state. These data were taken in a dry helium atmosphere. The hold time of the memory in air was considerably shorter.

We postulate that the memory device works by the injection of electrons from the SWNT into nearby trap states, either in the oxide or at the oxide surface. The sign of the threshold shift (positive with positive applied gate voltage) indicates that the effect is not due to trapped ions in the dielectric. The electric field at the SWNT when a bias of 10V is applied between SWNT and gate is on order 10^7V/cm, so charge transfer to the oxide may occur through corona discharge. The unusual charge storage mechanism in this device is possible because of the unusual construction of the device; unlike conventional semiconductor FETs, the semiconducting channel here is exposed and lies against the exposed surface of the gate dielectric.

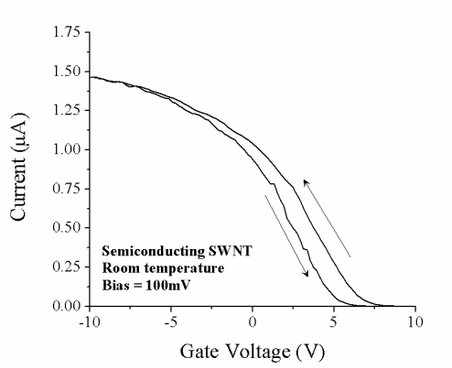

Fig. 1 Current as a function of gate voltage for a typical tubeFET device at room temperature with a source-drain bias of 100mV. Arrows indicate the sweep direction of the gate voltage.

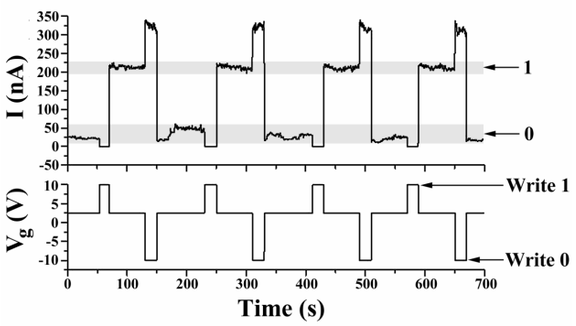

Fig. 2. Current and gate voltage as a function of time during several read/write/read/erase cycles of the tubeFET memory. 100mV source-drain bias was applied to the tubeFET.

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