Analytical Theory of the Ballistic Carbon Nanotube Field-Effect Transistor

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The rapid progress in carbon nanotube field-effect transistors (CNTFETs) (e.g. [1, 2]) creates a need for device simulations. Detailed numerical simulations will be useful, but there is also a need for simple, conceptual models to help interpret experiments and guide device design. In this talk, we present a new, analytical theory of the ideal CNTFET and use it to examine device performance limits and design issues.

For an ideal MISFET, the current is the product of the charge induced by the gate times the average carrier velocity. Traditional methods for MOS electrostatics [3] can be extended to CNTFETs to calculate the charge in the carbon nanotube (CNT). In brief, we use an effective mass level description of the CNT [4] and calculate the charge, Q_L, in the CNT for an assumed nanotube potential (ψ_S, or Fermi level). The corresponding gate voltage that produced this potential and charge is determined from

$$V_G = V_{fb} + \psi_S - Q_L / C_{ins}, \tag{1}$$

where C_{ins} is the nanotube to gate capacitance. Figure 1 shows a typical C_G vs. V_G characteristic, which reflects the 1D density of states (DOS) of the CNT. The charge induced in the CNT increases approximately linearly above threshold, as expected for an MIS capacitor.

Natori's 1D theory of the ballistic MOSFET [5] is readily extended to CNTFETs to calculate the average carrier velocity. In brief, positive k-states at the beginning of the channel are populated according to the source Fermi level and the negative k-states according to the drain Fermi level subject to the constraint that the total charge is fixed by MOS electrostatics as described above. Figure 2 shows a typical I_D vs. V_{DS} characteristic. The drain current saturation occurs when the drain bias is large so that no negative k-states are occupied. The inset shows that in contrast to the MOSFET, the channel conductance in a ballistic CNTFET is quantized. Figure 3, which shows log I_D vs. V_{GS} (left) and g_m vs. V_{GS} (right), shows that the ballistic CNTFET achieves an acceptable on-off ratio and a high transconductance, even at the low voltages needed to high-density systems.

The scaling limits of the CNTFET will be determined by 2D electrostatics, and scattering and parasitic resistance will likely limit the performance in practice. Nevertheless, the simple theory of the ideal CNTFET introduced here establishes for the first time upper performance limits and provides a useful guide for future work.

[1] V. Derycke, R. Martel, J. Appenzeller and Ph. Avouris, Nano Letters, **9**, 453 (2000).
[2] A. Bachtold, P. Hadley, T. Nakanishi and C. Dekker, Science, **294**, 1317 (2001).
[3] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices* (Cambridge University Press, Cambridge, UK, 1998).
[4] J. W. Mintmire and C. T. White, Phys. Rev. Lett., **81**, 2506 (1998).
[5] K. Natori, J. Appl. Phys., **76**, 4879 (1994).

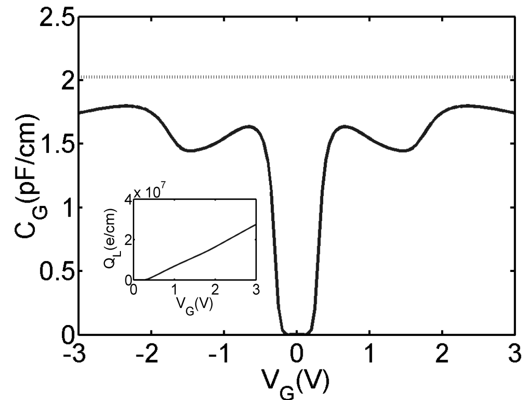

Fig. 1. Computed capacitance vs. gate voltage characteristic of a 1nm-diameter CNT with a 1nm (κ=4) insulator in a coaxial geometry at T=300K. The dotted line shows C_{ins}. The inset shows the nanotube charge vs. gate voltage characteristic.

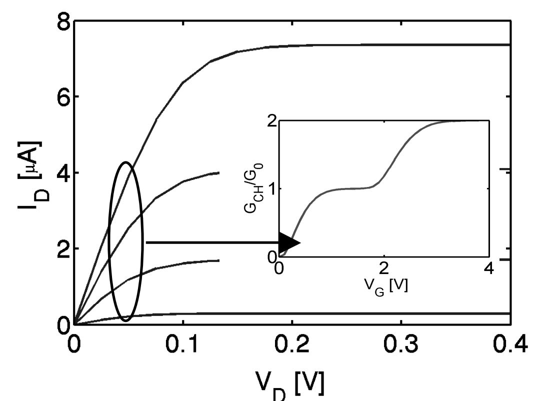

Fig. 2. Computed I_D vs. V_{DS} characteristic with gate bias as a parameter. (V_G=0.1-0.4V, 0.1V/step.) The inset shows the quantized channel conductance vs. gate voltage at $T = 300K$, where $G_0 = 4e^2/h$, and e is the electron charge and h the Planck constant.

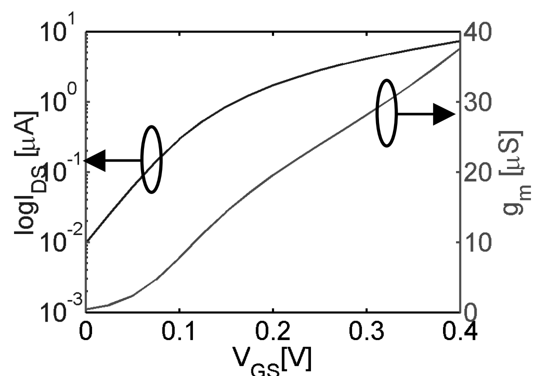

Fig. 3. Computed log(I_D) vs. V_{GS} characteristic (left) and transconductance vs. V_{GS} (right) at V_D=0.4V.