Properties of Thermally Evaporated HfO2

R. Garg, R.K. Jarwal, M. Bhaskaran,* P.K Swain* and D. Misra Department Electrical and Computer Engineering New Jersey Institute of Technology Newark, NJ 07102 *Sarnoff Corporation, Princeton, NJ 08543-5300

Compatibility with conventional CMOS process flows and a thermal budget up to 1000°C is critical for the successful introduction of high-k films. Recently, hafnium oxide (HfO_2) as high-k gate dielectrics has been under intense investigation for replacing conventional SiO₂ for its high dielectric constant (~20-25), low leakage current, and good thermal stability on silicon. Different methods such as ALD (atomic layer deposition) [1], CVD [2], and sputtering [3] have been used to grow hafnium oxide. Impact on interfaces seems to be the major concern in many of these growth techniques. In this work we have used thermal evaporation to grow HfO₂ since thermal evaporation is known to be a rather gentle process that creates none or very little damage to the interface.

500-angstrom HfO₂ films were grown on <100> ntype silicon wafers by using standard thermal evaporation of Hafnium while adding oxygen at constant partial pressure during evaporation. Before evaporation silicon wafers were cleaned using standard RCA cleans (RCA-1 and RCA-2) followed by 50:1 HF dip for 15 minutes immediately prior to HfO₂ growth. A lithography step was carried out to form metal oxide semiconductor capacitors with different diameters after depositing aluminum. Two different film thicknesses (500Å and 600Å) were considered for this work.

The 1 MHz *C-V* curves for the 500Å samples is shown in Fig. 1. High-*k* gate dielectrics show *C–V* hysteresis which lead to threshold voltage instability. Counterclockwise hysteresis for devices in Fig. 2 is attributed to several factors including damage caused during the HfO₂ and aluminum deposition and trapped charges Q_{ot} . Since the interfaces are less damaged for evaporated HfO₂ it can be attributed to oxide trapped charges in the bulk. When the devices were annealed at 350°C for 20 minutes hysteresis was reduced or eliminated.

ACKNOWLEDGEMENT

This work was partially supported by a grant from National Science Foundation (Award number 0140584).

REFERENCES

1. M. Tuominen et al, ECS PV 2000-9, 271-282 (2000).

2. S. J. Lee et al., 2001 Symposium on VLSI Technology, p. 133, 2001.

3. R. Nieh et al., Appl. Phys. Lett., vol 81(9), pp. 1663, 2002.

Fig. 1. Capacitance-voltage characteristic of thermally evaporated HfO_2 before post deposition annealing (PDA) shows strong hysteresis.

