ETCHING OF LOW-K INTERCONNECT MATERIALS FOR NEXT GENERATION DEVICES

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As integrated circuit device dimension are scaled down in the 0.1 µm dimension range, the line to line capacitance and line resistance of the metal interconnect increase the total resistance-capacitance (RC) delay of the signals during their propagation through different interconnect levels. Several solutions are being considered to reduce the RC delay. The solution is to replace the traditional aluminium and SiO_2 interconnect technology by copper and low permittivity constant dielectric materials (so called "low k"). Interconnection in integrated circuits is usually performed by deposition and patterning of a metal layer on the top of a dielectric material. Copper metallization is usually very difficult using this traditional metallization technology due to difficulties in etching Cu and contamination considerations. In order to solve this problem, a damascene technology is being used for Cu metallization. In the damascene approach, the dielectric is first deposited and the interconnect trenches and via are then defined by plasma etching. Copper is then deposited on the wafer which fills trenches and via. Many inorganic materials such as doped oxyde and organic materials are being investigated as potential candidates to replace SiO_2 in a damascene process (figure 1). The choice of a new dielectric has been and continues to be an exercise in trying to find the low k film with isotropic dielectric constant of less than 3, good thermal stability and adhesion on stop and barrier layers. At this time, there is no standard for these new materials and no material and deposition methods (CVD or Spin-on) have yet gained advantage. For low k materials (k<3) such as doped oxyde (SiOCH) or polymer (Silk^{TM}), etch processes have to be revisited to obtain adequate profile control in high aspect ratio structures, high etch rate and good selectivities to etch stop or hard mask such as SiO_2 (k = 3.9) and SiCH (k = 4). For the next low k generation (k<2.5) such as aerogels and porous polymers, the film becomes very sensitive to etch and strip processes due to the porosity. In most cases, the effect of this fragility is a structural modification of the low k as for instance uptake moisture which leads to an increase in the dielectric constant.

The etching of very high aspect ratio contact holes in hydrocarbon materials (Silk^{TM}) has been investigated in an industrial inductively coupled plasma using $O_2/N_2/CH_4$ gas feedstock. One of the major problem in the etching of Silk^{TM} is the formation of bow in high aspect ratio contact holes. The experimental results show that the bowing originates from the deflection of ions on the sidewalls, generating some etching. The mechanisms leading to ion distortion is mainly explained by differential charging on the feature sidewalls. XPS analysis reveals that profile control in the high aspect ratio contact holes is obtained thanks to the formation of a passivation layer on the polymer sidewalls preventing the spontaneous attacks by oxygen reactives species in the plasma. The presence of bow in high aspect ratio contact holes can be minimized and even suppressed in some cases by the formation of a thick passivation layer on the sidewalls during the etch process.

Etching of the low k SiOCH (BD^{TM}) and SiCH (etch stop) has been investigated in an industrial magnetically enhanced reactive ion etcher (MERIE). XPS on blanket wafers have been performed after partial etching in fluorocarbon based plasmas. During the etch, a steady state fluorocarbon layer (CFx) is present on the film surface, etch rate is governed by the balance of the neutral etchant flow through this layer and the etch by-product (SiFx) leaving the interaction layer. We observe that above a critical fluorocarbon thickness (3 nm) , the etch rate is strongly minimized. This thickness of 3 nm corresponds to the typical implantation depth of ions under our plasma operating conditions. This study shows that the oxygen and carbon content in the film plays a key role in controlling the fluorocarbon layer thickness and has consequently a direct impact on the etching performance. *A priori* knowledge of material composition and characterization of the response to typical fluorocarbon plasma etch can help in the engineering definition of the best stack for low k integration.

Figure 1 : Dielectric materials as candidates for low k