

Study of Effect of Plasma Etching on LER

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The 2001 ITRS defines LER as “the local line width variation (3sigma total, all frequency components included, both edges) evaluated along a distance equal to four times the technology node.” LER has been correlated to increase of leakage current of sub-100 nm transistor performance [1] and is an increasing issue with 193 nm resist. [2] This paper describes study of the effect of plasma etching process on LER. Initial experiments have shown the reduction in the LER value in the final etched features (130 nm trenches in oxide), as compared to LER measured on the resist.

The review of the present literature shows that LER value depends on the size of the measurement window. [3] The current theories believe that resist LER is from the structures at molecular level contributions from polymer aggregates, more than 30 nm in diameter, in the resist material. [7] It has also been noted that due to decreasing feature size, it results from increased sensitivity to statistical fluctuations inherent in chemically amplified resist: exposure, acid release and post exposure bake process. [6] It is also important to note that the surface roughness and the line edge roughness of resists are related [6]. Initial measurements have shown the dependence of LER on PEB, PAB and develop time is also noted. [6] The values of LER decreased when we used a chemically amplified resist, consisting of base polymer with a high molecular weight and photo-acid generator producing acid with a high molecular weight. [4,5] Addition sources of origination are attributed to reticle (low-frequency contribution) and resist process (high frequency component). [10]

In order to study the effect of LER on the etch process, we measured the LER for RCD and monitored the LER as a function of BARC etch, electrode temperature, RF power and etch time. Trenches were patterned with a 193 nm resist and etched stack was PECVD oxide stopping on nitride. Target value for RCD was 130 nm. Initial measurements show that value of LER decreases with the decreasing lower electrode temperature, as shown in figure 1.

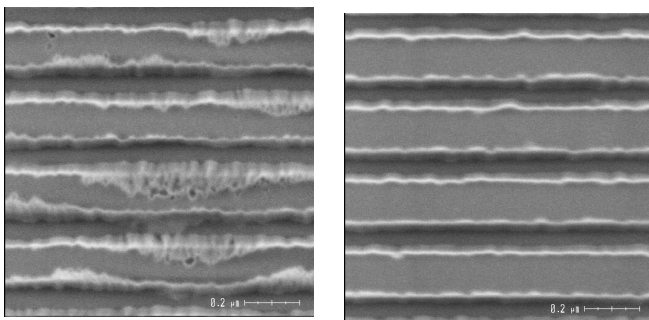


Figure 1: SEM cross-section of 130 nm trenches. SEM on the left shows a structure etched with an electrode temperature of 60C (3 sigma LER of 14.5 nm) while SEM on the right shows the SEM for the wafer etched with a lower electrode temperature of 20C. (3 sigma LER of 5 nm) nm.

We also noted that LER decreased in the etched features as compared to resist LER. We started with LER of 9.6 nm with 3.8 nm of SD and achieved on the final process LER value of 5 nm with SD of 1.4 nm. It was also observed that as the etch process progresses the value of LER first drops quickly and then start to increase again as more of the pattern from resist is transferred to the bottom oxide. Over etch, from 100 to 125 s of etch, contributed to LER as all of the resist was etched away .

Table 1: LER as a function of etch time

Etch Time (s)	LER (3 Sigma) (nm)	SD (nm)
RCD	9.6	3.8
50	4.2	0.82
75	4.77	0.99
100	5.12	1.4
125	6.35	4.96

It was also observed in the experiments that LER decreases with decreasing RF power. When we etched all wafers for 100s using the same conditions, and varied the RF power, LER decreased as the RF power was lowered.

In the full paper results will presented on the effect of etch chemistry on the LER in addition to further experimental details and additional data from the study.

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References:

- [1] “ Experimental Determination of the Impact of Polysilicon LER on sub-100 nm transistor Performance,” *Metrology, Inspection and Process Control for Microlithography XV*, SPIE vol. 4344, 2001, pp. 809-814. K Patterson et al. and references therein.
- [2] “193nm resists: A status report- (Part Two),” by E. Richter et al, *Future Fab International*, Issue 13, 2002
- [3] G. Eytan et al., *Proc. SPIE 4869*, (2002), to be published.
- [4] “Reduction of Line edge Roughness in the top-surface imaging process,” Shigeyasu Mori et al, *J. Vac. Sci. technol. B 16 (6)*, pp. 3739, Nov/Dec 1998.
- [5] “Top Surface imaging process and material development for 193 nm and extreme ultraviolet lithography,” Veena Rao et al, *J. Vac. Sci. technol. B 16 (6)*, pp. 3722, Nov/Dec 1998.
- [6] “Continuum model of Shot Noise and Line Edge Roughness,” G. M. Gallatin, *Lithography for Semiconductor Manufacturing II*, Chris A. Mack, Tom Stevenson, Editors, *Proceedings of SPIE Vol. 4404*, pp. 123-132, 2001.
- [7] “Influence of Edge Roughness in resist Patterns on Etched Patterns,” Hideo Namatsu et al, *J. Vac. Sci. technol. B 16 (6)*, pp. 3315 Nov/Dec 1998.
- [8] “Simulation of Surface and line-edge roughness formation in resists,” G. P. Patsis et al, *Microelectronics Engineering 57-58*, pp. 563-569, 2001.
- [9] S. C. Palmateerr et al., *Proc. SPIE*, pp. 3333, 634, 1998.
- [10] T. Yamaguchi et al., *Proc. SPIE*, pp. 3678, 617, 1999