ECD SEED™ COPPER LAYER FOR SEED ENHANCEMENT IN ADVANCED INTERCONNECTS

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Introduction

With progress of ultra large-scale integration (ULSI), RC delay issues in interconnects have driven the emergence of copper as a conductive material [1]. With the use of copper, process evolution was necessary and led to the development of the damascene architecture, which consists of depositing and patterning dielectric before copper filling of the features by electrochemical deposition (ECD) [2].

As feature size further shrinks, seed layer deposition for efficient electroplating becomes a critical step in this sequence. PVD techniques, which lead to non- conformal deposits, will probably reach their limits with the 90 nm node; with feature size reduction very thin PVD seed layers will be required, which are likely to be discontinuous inside the features (Figure 1).

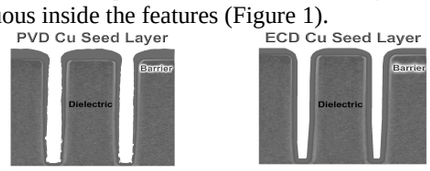

Figure 1: *seed layer enhancement using the ECD Seed process.*

A promising solution to push the limits of PVD seed layer has been proposed, which consists of recovering seed layer integrity by electrodeposition means using the ECD Seed process [3] (Figure 1). The purpose of this article is to present results obtained in an evaluation of this process carried out using Semitool's Paragon® system. Electrochemical, microstructural and integration aspects will be discussed.

Electrochemical study

Polarization curves and quartz microbalance measurements were performed at the laboratory scale (Figure 2). They showed that under anodic conditions, the copper surface is not dissolved. Similarly, copper etching rates in the ECD Seed chemistry are very low, ensuring efficient seed layer protection in the first seconds of deposition.

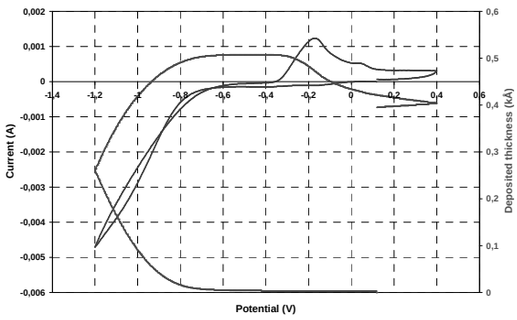

Figure 2: *polarization curve and quartz microbalance measurements*

Cathode efficiency measurements performed on full size wafers revealed an efficiency of copper deposition of 90%. Moreover, copper density was found to be ~8g/cm^3.

For practical purposes, film uniformity across the wafer is a critical parameter. Using the CFD reactor, non-uniformities as low as σ=1.1% were obtained on 800 Å ECD Seed layers.

ECD Seed layer characterization

ECD Seed copper layers were successfully deposited on blanket wafers covered with both non-collimated and SiP PVD seed layers and TiN or TaN/Ta diffusion barriers. Efficient deposition was achieved using seed layers as thin as 80 Å. Stress measurements and X-Ray diffraction (XRD) experiments evidenced that ECD Seed copper behaves like standard ECD copper. The slight as-deposited tensile stress drastically increases after anneal, and a strong (111) texture is observed on TaN/Ta barrier layers, whereas no significant texture is observed with TiN. As-deposited grain size was estimated to be 200 Å. X-Ray reflectometry (XRR) measurements confirmed the lower copper density, and provided roughness values of a few nm, in good agreement with AFM observations.

ECD Seed integration

To assess integration capabilities of this process, a morphological study of trench step coverage was undertaken. Successful deposition was achieved on 150-200 Å seed layers. SEM observations evidenced that ECD Seed deposits are essentially conformal. Using 400 Å layers, efficient step coverage is obtained (Figure 3), which should lead to efficient feature filling by ECD.

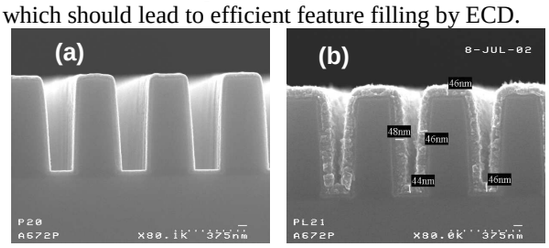

Figure 3: *PVD 150 Å (a) and PVD 150 Å + ECD Seed 400 Å (b)*

Conclusion

In this article, we have presented promising results concerning seed enhancement by the ECD Seed process for advanced interconnects. Thanks to favorable electrochemical properties, this solution proved to be efficient to achieve deposition on very thin and discontinuous seed layers. Copper films have been characterized, and should be suitable for efficient feature filling for the 90 nm node and below.

References

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