INTRODUCING ADVANCED ULK DIELECTRIC MATERIALS IN INTERCONNECTS: PERFORMANCE AND INTEGRATION CHALLENGES

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Abstract

In this communication, we will review critical points related to Ultra low K (ULK) integration and possible solutions to solve major issues. To further understand those advanced materials behaviors during architecture construction and validate the proposed integration schemes, new characterization methodologies are required and thus introduced.

Introduction

To further reduce RC delays, power consumption and cross-talk and thus achieve performance improvements moving below 90 nm node in multilevel copper interconnect Dual Damascene schemes, Ultra Low K (ULK) materials with dielectric constant, K close or less than 2.2 attract much attention. Today, two deposition approaches are under investigation : spin-on and CVD, but most of porous materials are spin-on coated. Even if aromatic polymers are available on the market, the materials that looks most promising to combine the high thermal stability of silica with the lowest achievable dielectric constant is likely nano-porous SiOC films. The idea of lowering the K value by decreasing the density can be taken one step further by introducing organic materials [1] by creating voids into the film using a porogen approach with either spin on deposition [2, 3] or Plasma Enhanced Chemical Vapor Deposition (PECVD). Indeed, the ability to prepare porous ULK materials using a porogen approach combined with PECVD deposition is now a new realistic approach. In addition of thermal curing usually employed to remove the sacrificial compounds, several post-treatments were therefore imagined as H_2 plasma or supercritical CO_2 process.

ULK process compatibility with integration

The integration and process stabilization of copper /low K (K = 3.0) interconnect in Dual Damascene architecture for 90 nm node technology (300 mm wafer size) remains today a challenge. Therefore, introducing porous materials into advanced interconnect fabrication induces further more challenges. One can report, for instance, two identified issues which are: moisture uptake or chemicals absorption due to porosity and mechanical fragility (materials are soft or brittle).

Novel schemes are accordingly required to enable integration of materials with K < 2.5 to achieve the lowest effective permitivity of the integrated structure including the necessary dielectric barriers and liners. These requirements drive the development of new low K Cu barriers such as SiC derivatives to replace or improve actual materials also employed for etch stop and hard mask applications. In the same time, timed etches have been developed to eliminate the use of a mid etch stop layer.

In addition, due to a high Cu diffusion rate, a diffusion barrier is needed, the integrity of this barrier being an important issue. Owing to its high resistiviy relatively to copper, its thickness should be the thinner as possible without compromising its integrity. Different materials (TaN, TiN, TiNSi…) and deposition techniques (PVD, CVD, ALD…) are in competition to provide the lower barrier resistivity, a good step coverage and a good Cu barrier diffusion. Some previous results have shown that more than 30 nm of physical vapor deposited (PVD) Ta(N) are necessary to provide a continuous barrier on a porous ULK [4]. More recently, some integrity measurements were reported on chemical vapor deposited (CVD) TiN barrier processed on a porous SiOC using spectroscopic ellipsometry coupled with solvent absorption [5]. A 10 nm CVD TiN was shown to be required for a continuous layer. Another possible issue of porous ULK integration is a non negligible diffusion of gas precursor in the open porosity of the ULK as it was demonstrated by EDAX or EELS (Fig. 1).

Mechanical Behavior

Increasing interconnects metal levels (> 10) and introducing ULK materials with mechanical properties drastically affected by porosity can lead to severe CMP and packaging failure. Both ULK mechanical properties (hardness, modulus…) and adhesion strength between dielectric or metallic layers must therefore be considered since cracks can occur due to multi-stack global stress or wire-bonding (Fig. 2). While the first insures the capability of the material to support all the process steps including metal re-crystallization and packaging, the latter insures stack stability during local or global stress variations including thermal treatments or process such as CMP. ULK post-curing such as H_2 or E-beam are today under investigation to improve mechanical properties and adhesion is suggested to be increased using several surface plasma treatments (Fig. 3).

Conclusion

Ultra Low K materials with porous scheme need special process adjustment to successful their integration with copper in damascene structure. This leads to introduce new techniques both for integration process steps and characterization.

References

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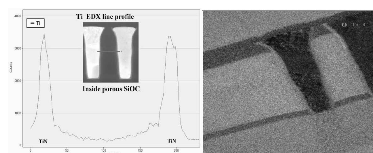

Figure 1: CVD TiN on porous SiOC EDX and EELS analysis

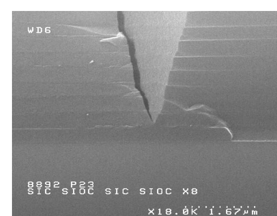

Figure 2: SEM of a SiOC-SiC multi-layer cracking

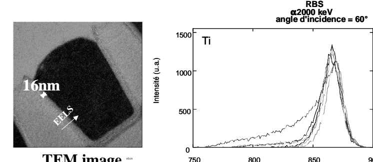

Figure 3: CVD TiN on porous SiOC TEM and RBS analysis