Industry Challenges in Post-Etch Cleaning Chemistries for Advanced Copper/Low-κ Applications

Michael A. Fury
DuPont EKC Technology
1320 El Capitan Drive
Danville, CA 94526 USA
mfury@ekctech.com

The semiconductor industry migration from aluminum and tungsten interconnects to copper interconnects with low-κ dielectrics presents a multitude of both opportunities and challenges to chip manufacturers and to the suppliers of materials and processing equipment. The present change in interconnect materials set is concurrent with continuing device shrinkage that is driving a change in lithography technology and photoresist materials. These changes are further complicated by the concurrent migration from 200mm to 300mm manufacturing for leading edge devices. In the previous major interconnect migration from all-aluminum wiring to aluminum lines with vertical tungsten plugs, the industry rapidly converged on a consistent interconnect structure, barrier metallurgy, and the dielectric of choice remained SiO_2.

In the present migration, the industry has converged on dual damascene electroplated copper with a tantalum-based barrier, but has splintered in its choice of low-κ dielectrics. This fractious market creates a significant set of challenges for the cleaning of post-etch residues. Copper is more readily oxidized than aluminum, thus restricting the use of conventional post-etch residue removers such as hydroxylamine. The disparity of chemical compositions of the low-κ dielectrics forces further compatibility restrictions on the remover chemistry. Unlike the SiO_2 case, however, the remover suppliers have needed to respond with a range of formulations unique to each dielectric family, and often unique to each customer. This formulation development must be completed early in the integration development process for the low-κ dielectric, in order for feasibility of that dielectric to be validated. Since the integration process can often lead to failure of the dielectric, the effort expended on remover development is unable to provide a return on investment to the supplier.

Another critical process & structure element introduced in the copper damascene era is the presence of a bottom anti-reflective coating (BARC) layer. This non-reflective layer is deposited in the stack to improve lithography performance, and must be removed following trench and via etch and prior to barrier and copper metal deposition. Removal of these BARC materials provides another degree of difficulty for establishing a viable manufacturing process flow.

The dimensions at which copper and low-κ dielectrics become critical to device performance require that lithography be performed at the 248nm exposure wavelength. The deep ultra-violet (DUV) photoresists required for such processing are extremely sensitive to the presence of amines, which can induce cross-linking in the photoresist at sub-ppm levels. It is thus necessary to prohibit residue removal chemistries that contain amines, even though these formed the basis for most successful remover formulations in the prior device generations.

Environmental regulations around the globe are inconsistent from one semiconductor manufacturing region to another. Given the intricate network of technology transfer partnerships in the semiconductor industry, it is incumbent on chemical formulators in any one region to be responsive to the regulatory restrictions in other regions, even if the proposed formulation is acceptable in the immediate circumstance. This serves to further constrain the options available to the wafer cleaning formulator.

Environmental concerns also promote a trend away from solvent-based cleaning systems toward water-based systems, particularly those with low concentrations of chemicals. Post-etch residues are rarely water soluble in their own right, and require some significant amount of coaxing to relinquish their grip on the device features. Identifying chemistries that can be simultaneously aggressive, non-corrosive, inexpensive and environmentally benign has proven to be an elusive task, although some promising options have been demonstrated, even if only for a limited range of process conditions.

At the same time, economic forces are driving the introduction of 300mm tools at the same technology nodes for which copper and low-κ dielectrics become critical to device performance. The majority of wafer cleaning equipment sold into the early 300mm fabs consisted of conventional wet benches for batch processing. However, the equipment suppliers are promoting a transition to a variety of cleaning technology alternatives that operate in a single wafer mode. The immediate impact of this transition on the cleaning chemistry is that the cycle time available to each wafer must be dramatically reduced in order to maintain a cost-effective throughput at the process sector level. This demand for faster, more aggressive formulations is in direct conflict with the compatibility restrictions created by the copper, barrier, low-κ dielectric and BARC materials. It is clear that the operating space for a fast, defect-free cleaning process is shrinking.

This talk will review the rapid evolution of post-etch residue removal chemistries from the introduction of copper designs to the present day. The influence of equipment design on chemistry and process parameters will be discussed. Several critical issues facing the process integrator have been addressed successfully; several more remain to be solved. The presentation will conclude with a brief look at emerging technologies for bulk photoresist stripping and post-etch residue removal.

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